

# LS TTL Data

**ON Semiconductor**  
*Formerly a Division of Motorola*



# LS TTL Data

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Formerly Titled "FAST and LS TTL Data"


**Please Note:** As ON Semiconductor has exited the FAST TTL business, all FAST data sheets have been removed from this publication. For further assistance, please contact your local ON Semiconductor representative.

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**CHAPTER 1**  
**Selection Information**  
**LS TTL**

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## GENERAL INFORMATION

### TTL in Perspective

Since its introduction, TTL has become the most popular form of digital logic. It has evolved from the original gold-doped saturated 7400 logic, to Schottky-Clamped logic, and finally to the modern advanced families of TTL logic. The popularity of these TTL families stem from their ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Low Power Schottky (LSTTL) was the industry standard logic family for many years. Since its inception, several more modern families have come out, with equal or better

performance. We therefore recommend the VHC, High Speed and FACT products for all new 5.0 Volt designs. Further improvements in power reduction can be achieved using the LVX, LCX or VCX running at 3.3 Volts. Improvements in electrostatic discharge susceptibility in these newer CMOS products now make them obviate the need for LSTTL in new designs. The VHC family is faster and lower power with similar drive characteristics compared to LSTTL. We highly recommend new designs use one or more of these CMOS families.

### TTL Family Comparisons

#### General Characteristics for Schottky TTL Logic (All Maximum Ratings)

Characteristic	Symbol	74LSxxx	Unit
Operating Voltage Range	$V_{CC}$	$5 \pm 5\%$	Vdc
Operating Temperature Range	$T_A$	0 to 70	°C
Input Current	$I_{IN}$	$I_{IH}$	20
		$I_{IL}$	-400
Output Drive Standard Output	$I_{OH}$	-0.4	mA
	$I_{OL}$	8.0	mA
	$I_{SC}$	-20 to -100	mA
Buffer Output	$I_{OH}$	-15	mA
	$I_{OL}$	24	mA
	$I_{SC}$	-40 to -225	mA

#### Speed/Power Characteristics for Schottky TTL Logic<sup>(1)</sup> (All Typical Ratings)

Characteristic	Symbol	Typ	Unit
Quiescent Supply Current/Gate	$I_G$	0.4	mA
Power/Gate (Quiescent)	$P_G$	2.0	mW
Propagation Delay	$t_p$	9.0	ns
Speed Power Product	—	18	pJ
Clock Frequency (D-F/F)	$f_{max}$	33	MHz
Clock Frequency (Counter)	$f_{max}$	40	MHz

NOTES: 1. Specifications are shown for the following conditions:

- a)  $V_{CC} = 5.0$  Vdc (AC),
- b)  $T_A = 25^\circ\text{C}$ ,
- c)  $C_L = 15$  pF.

## Functional Selection

### Abbreviations

S = Synchronous  
 A = Asynchronous  
 B = Both Synchronous and Asynchronous

2S = 2-State Output  
 3S = 3-State Output  
 OC = Open-Collector Output

### Inverters

Description	Type of Output	No.
Hex	2S	04
	OC	05

### AND Gates

Description	Type of Output	No.
Quad 2-Input	2S	08

### NAND Gates

Description	Type of Output	No.
Quad 2-Input	2S	00

### OR Gates

Description	Type of Output	No.
Quad 2-Input	2S	32

### NOR Gates

Description	Type of Output	No.
Dual 5-Input	2S	260

### Exclusive OR Gates

Description	Type of Output	No.
Quad 2-Input	2S	86

### Schmitt Triggers

Description	Type of Output	No.
Hex, Inverting	2S	14
Quad 2-Input NAND Gate	2S	132

### SSI Flip-Flops

Description	Clock Edge	No.
Dual D w/Set & Clear	Pos	74A
Dual JK w/Set & Clear Individual J, K, C <sub>P</sub> , S <sub>D</sub> , C <sub>D</sub> Inputs	Neg	76A
Dual JK w/Set & Clear	Pos	109A

### Multiplexers

Description	Type of Output	No.
Quad 2-to-1, Non-Inverting	2S	157
	3S	257B
Quad 2-to-1, Inverting	3S	258B
	2S	153
Dual 4-to-1, Non-Inverting	3S	253
	2S	151
8-to-1	3S	251
	2S	298

### Encoders

Description	Type of Output	No.
10-to-4-Line BCD	2S	147
8-to-3-Line Priority Encoder	2S	148

### Register Files

Description	Type of Output	No.
4 x 4	3S	670

### Decoders/Demultiplexers

Description	Type of Output	No.
Dual 1-of-4	2S	139
	OC	156
1-of-8	2S	138
1-of-10	2S	42

### Latches

Description	No. of Bits	Type of Output	No.
Transparent, Non-Inverting Addressable	8	3S	373
	8	2S	259



## Shift Registers

Description	No. of Bits	Type of Output	Mode*				No.
			SR	SL	Hold	Reset	
Serial In-Parallel Out	8	2S	X			A	164
Parallel In-Serial Out	8	2S	X		X		165
	8	2S	X		X	A	166
Parallel In-Parallel Out	4	2S	X	X	X	A	194A
	4	2S	X			A	195A
Parallel In-Parallel Out, Bidirectional	8	3S	X	X	X	A	299

\* SR = Shift Right  
SL = Shift Left

## Asynchronous Counters — Negative Edge-Triggered

Description	Load	Set	Reset	No.
Dual 4-Bit Binary			X	393

\* The 716 and 718 are positive edge-triggered.

## Display Decoders/Drivers with Open-Collector Outputs

Description	No.
1-of-10	145
BCD-to-7 Segment	247

## Cascadable Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.
4-Bit Binary	2S	S	A	161A
	2S	S	S	163A

## MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.
D-Type, Non-Inverting	4	2S		X	377
	6	2S	A		174
	8	2S	A		273
	8	3S			374
D-Type, Q and $\bar{Q}$ Outputs	4	2S	A		175

## Arithmetic Operators

Description	No.
4-Bit Adder	283

## Magnitude Comparators

Description	Type of Output	P = Q	P > Q	P < Q	No.
4-Bit	2S	X	X	X	85
8-Bit	2S	X	X		682
	2S	X	X		684
8-Bit with Output Enable	2S	X			688

## Parity Generators/Checkers

Description	No.
9-Bit Odd Even Parity Generator Checker	280

## VCOs and Multivibrators

Description	No.
Retriggerable Monostable Multivibrator	122
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Precision Non-Retriggerable Monostable Multivibrator	221

## Buffers/Line Drivers

Description	Type of Output	No.
Quad 2-Input NAND	OC	38
Quad, Non-Inverting	3S	125A
		126A
Hex, Non-Inverting	3S	365A
		367A
Hex, Inverting		368A
Octal, Non-Inverting	3S	244
Bus Pinout	3S	541
Octal, Inverting	3S	240

## Transceivers

Description	Type of Output	No.
Octal, Non-Inverting	3S	245
	OC	641
Octal, Inverting	3S	640
	OC	642

## **CHAPTER 2**

# **Circuit Characteristics**

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# CIRCUIT CHARACTERISTICS

## FAMILY CHARACTERISTICS LS TTL

The Low Power Schottky (LS TTL) family combines a current and power reduction improvement over standard 7400 TTL by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing.

## CIRCUIT FEATURES

Circuit features of the LS are best understood by examining the TTL 2-input NAND gate (Figure 1). While LS has been a popular series in the past, more modern products such as VHC should be replacing LSTTL in new designs. For applications where high drive is required, FACT is an ideal choice.

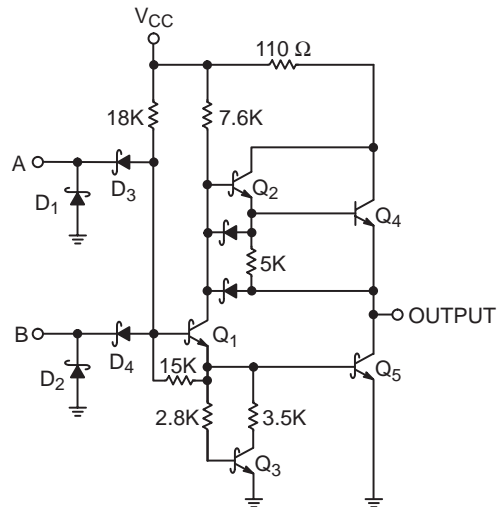


Figure 1. LS00 — 2-Input NAND Gate

## INPUT CONFIGURATION

ON Semiconductor LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in Figure 1. Compared to the classical multi-emitter structure, this circuit is faster and increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 7.0 V and the input breakdown voltage is typically 15 V or more.

Another input arrangement often used in LS MSI has three diodes connected as shown in Figure 2. This configuration gives a slightly higher input threshold than that of Figure 1. A third input configuration that is sometimes used in LS TTL employs a vertical PNP transistor as shown in Figure 3. This arrangement also gives a higher input threshold and has

the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 7.0 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in Figure 1. These diodes conduct when an input signal goes negative, which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2.0 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of an LS circuit and thus cause logic errors.

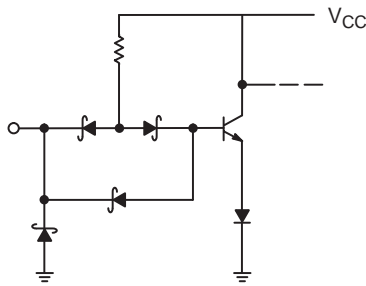


Figure 2. Diode Cluster Input

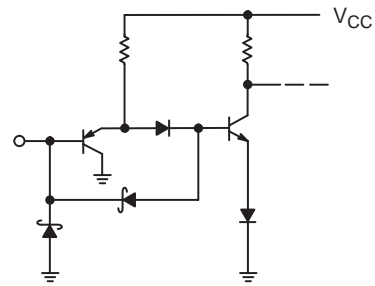


Figure 3. PNP Input

## INPUT CHARACTERISTICS

Figure 4 shows the typical input characteristics of LS. Typical transfer characteristics can be found in Figure 5 and

input threshold variation with temperature information is provided in Table 1.

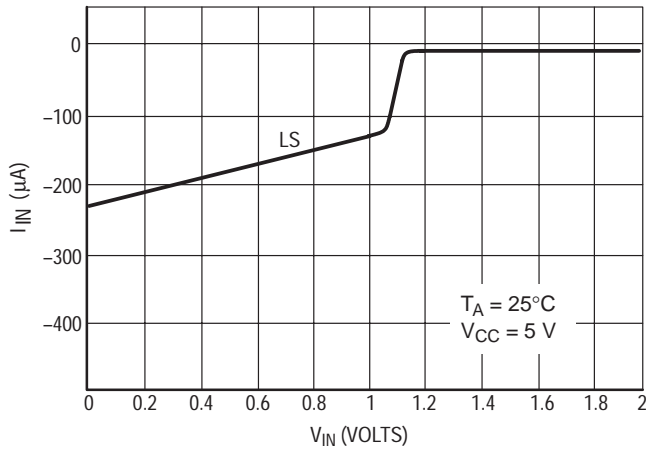


Figure 4. Typical Input Current versus Input Voltage

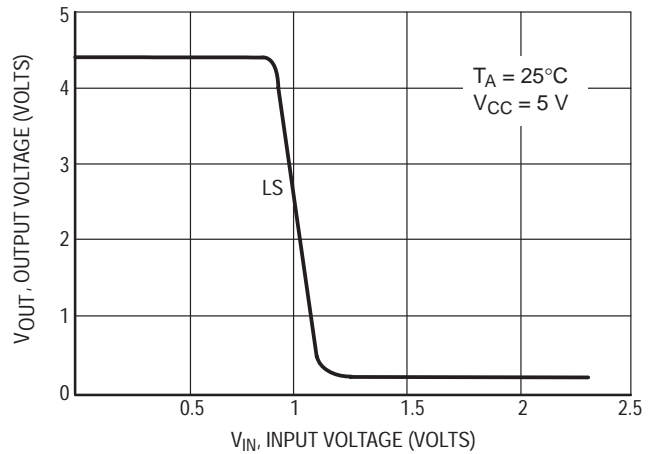


Figure 5. Typical Output versus Input Voltage Characteristic

Table 1. Typical Input Threshold Variation with Temperature

	-55°C	+25°C	+125°C
ALS	1.8	1.5	1.3
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

## OUTPUT CONFIGURATION

The output circuitry of LSTTL has several features not found in conventional TTL. A few of these features are discussed below.

Referring to Figure 1, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (Figure 5) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through

a 5.0K resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one  $V_{BE}$  below  $V_{CC}$  for low values of output current.

Figure 6 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is HIGH, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of two or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

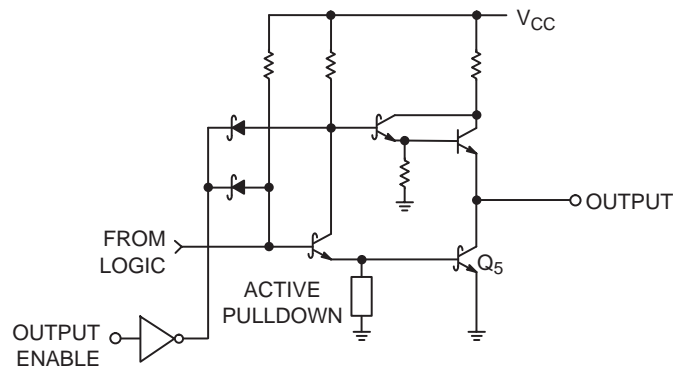


Figure 6. Typical 3-State Output Control

## OUTPUT CHARACTERISTICS

Figure 7 shows the LOW-state output characteristics for LS. For LOW  $I_{OL}$  values, the pull-down transistor is

clamped out of deep saturation to shorten the turn-off delay. Figure 8 shows the HIGH-state output characteristics.

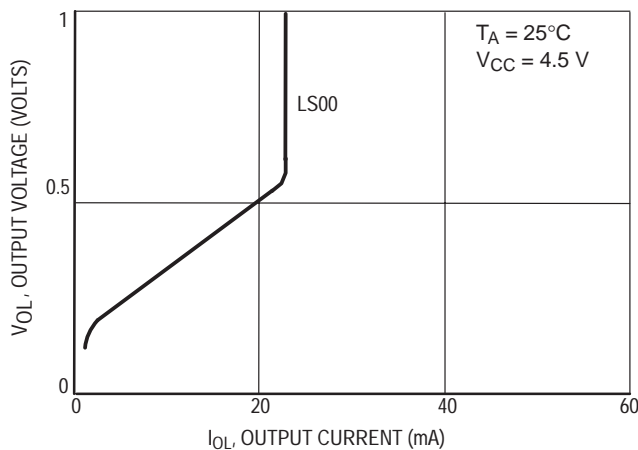


Figure 7. (a) Output Low Characteristic

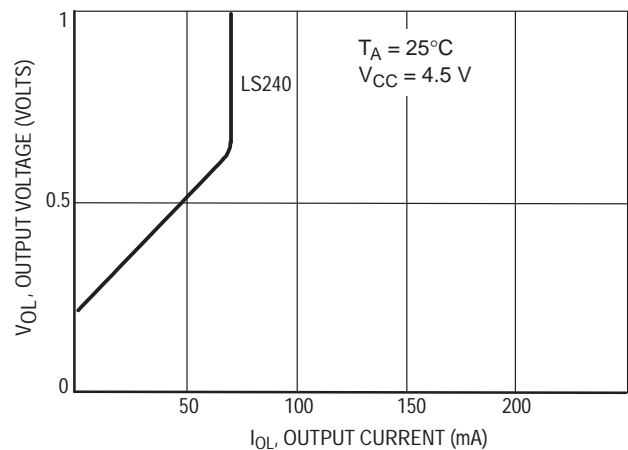


Figure 7. (b) Output Low Characteristic

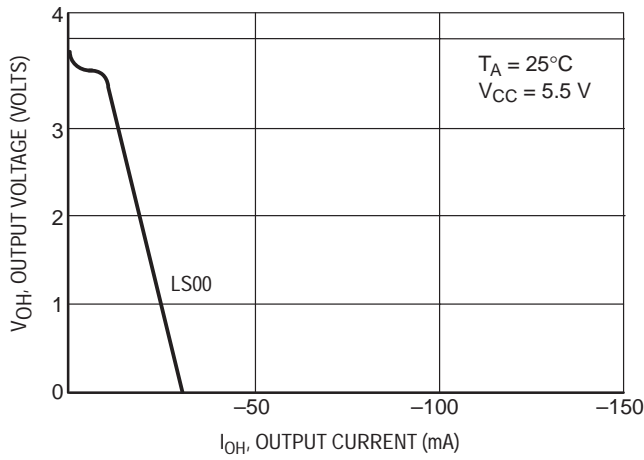


Figure 8. (a) Output High Characteristic

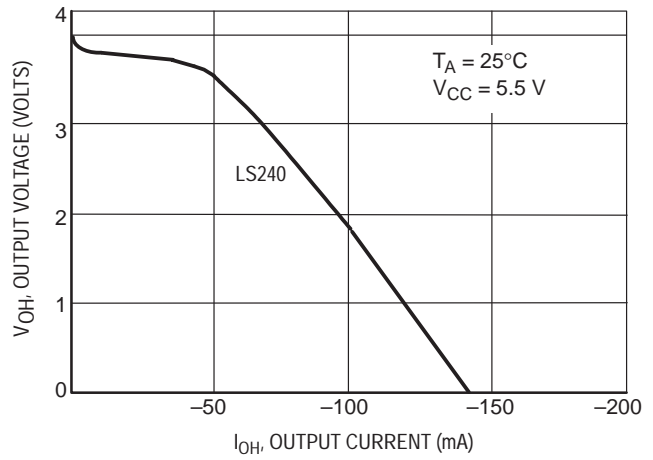


Figure 8. (b) Output High Characteristic

**AC SWITCHING CHARACTERISTICS**

The propagation through a logic element depends on power supply voltage, ambient temperature, and output load. The effect of each of these parameters on ac propagation is shown in Figures 9 through 11.

Propagation delays are specified with only one output switching, the delay through a logic-element will increase to some extent when multiple outputs switch simultaneously due to inductance internal to the IC package.

For LS TTL, limits are guaranteed at 25°C, V<sub>CC</sub> = 5.0 V, and C<sub>L</sub> = 15 pF (normally, resistive load has minimal effect on propagation delay) TTL limits are guaranteed over the commercial or military temperature and supply voltage ranges and with C<sub>L</sub> = 50 pF.

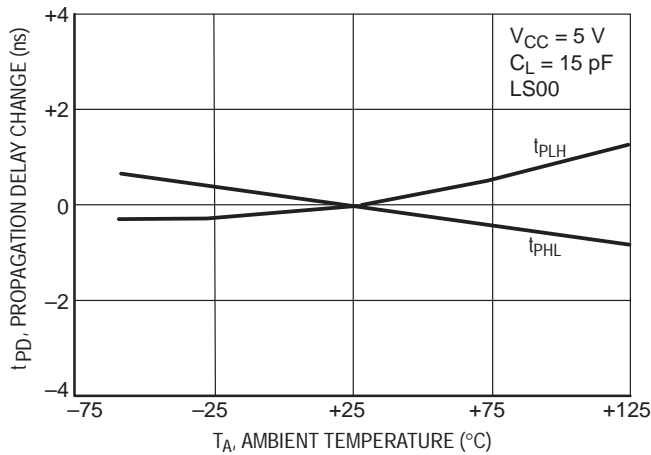


Figure 9.

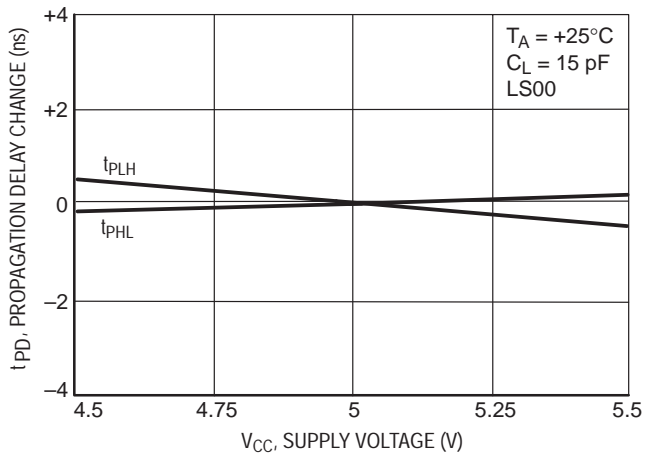
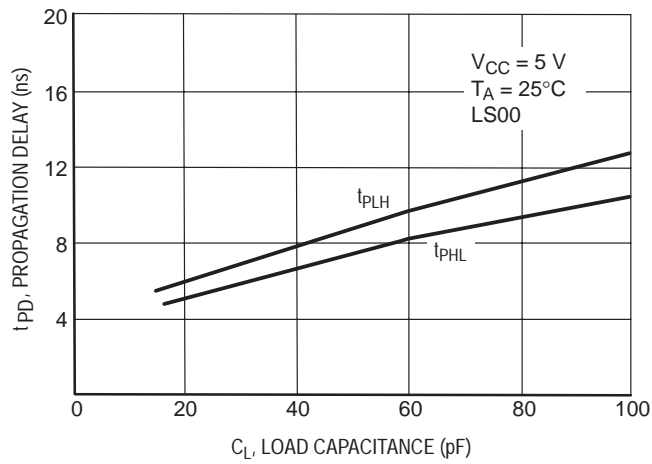


Figure 10.



\*Data for Figure 11 was taken with only one output switching at a time.

**Figure 11. \***

**ESD CHARACTERISTICS**

Electrostatic Discharge (ESD) sensitivity for ON Semiconductor TTL is characterized using several methodologies (HBM, MM, CDM). It is extremely important to understand that ESD sensitivity values alone are not sufficient when comparing devices. In an attempt to reduce correlation problems between various pieces of test equipment, all of which meet Mil-Std-883C requirements, tester specific information as well as actual device ESD

hardness levels are given in controlled documents and are available upon request. The continuing improvements of ESD sensitivity through redesigns of ON Semiconductor TTL has resulted in minimum ESD levels for all new products and redesigns of >3500 volts for LS. For device specific values reference the following specification:

LS: 12MRM 93831A

**CHAPTER 3**  
**Design Considerations**  
**Testing and Applications Assistance Form**

---



## DESIGN CONSIDERATIONS

### NOISE IMMUNITY

When mixing TTL families it is often desirable to know the guaranteed noise immunity for both LOW and HIGH logic levels. Table 2 lists the guaranteed logic levels for various TTL families and can be used to calculate noise margin. Table 3 specifies these noise margins for systems

containing LS, S, and/or ALS TTL. Note that Table 3 represents “worst case” limits and assumes a maximum power supply and temperature variation across the IC’s which are interconnected, as well as maximum rated load. Increased noise immunity can be achieved by designing with decreased maximum allowable operating ranges.

**Table 2.**  
**Worst Case TTL Logic Levels**

#### Electrical Characteristics

	TTL Families	Military (–55 to +125°C)				Commercial (0 to 70°C)				Unit
		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>OL</sub>	V <sub>OH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>OL</sub>	V <sub>OH</sub>	
TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
HTTL	High Speed TTL 54/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LPTTL	Low Power TTL 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
STTL	Schottky TTL 54/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LSTTL	Low Power Schottky TTL 54/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V
ALS TTL	(5% V <sub>CC</sub> ) (10% V <sub>CC</sub> ) Advanced LS TTL, 54/74ALS	0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.75	V
		0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.5	V

V<sub>OL</sub> and V<sub>OH</sub> are the voltages generated at the output V<sub>IL</sub> and V<sub>IH</sub> are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

**Table 3. (a)**  
**LOW Level Noise Margins (Commercial)**

From	To				Unit
		LS	S	ALS	
LS		300	300	300	mV
S		300	300	300	mV
ALS		300	300	300	mV

From “V<sub>OL</sub>” to “V<sub>IL</sub>”

**Table 3. (b)**  
**HIGH Level Noise Margins (Commercial)**

From	To				Unit
		LS	S	ALS	
LS		700	700	700	mV
S		700	700	700	mV
ALS (5% V <sub>CC</sub> )		750	750	750	mV
ALS (10% V <sub>CC</sub> )		500	500	500	mV

From “V<sub>OH</sub>” to “V<sub>IH</sub>”

### POWER CONSUMPTION

With the exception of ECL, all logic families exhibit increased power consumption at high frequencies. Care must be taken when switching multiple gates at high frequencies to assure that their combined dissipation does not exceed package and/or device capabilities. TTL devices are more efficient at high frequencies than CMOS.

### FAN-IN AND FAN-OUT

In order to simplify designing with ON Semiconductor TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA in the HIGH state (Logic “1”)
1 TTL Unit Load (U.L.) = 1.6 mA in the LOW state (Logic “0”)

Input loading and output drive factors of all products described in this handbook are related to these definitions.

**EXAMPLES — INPUT LOAD**

1. A 7400 gate, which has a maximum  $I_{IL}$  of 1.6 mA and  $I_{IH}$  of 40  $\mu$ A is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95B which has a value of  $I_{IL} = 0.8$  mA and  $I_{IH}$  of 40  $\mu$ A on the CP terminal, is specified as having an input LOW load factor of:

$$\frac{0.8 \text{ mA}}{1.6 \text{ mA}} \text{ or } 0.5 \text{ U.L.} \quad \text{and an input HIGH load factor of} \quad \frac{40 \mu\text{A}}{40 \mu\text{A}} \quad \text{or } 1 \text{ U.L.}$$

3. The 74LS00 gate which has an  $I_{IL}$  of 0.4 mA and an  $I_{IH}$  of 20  $\mu$ A, has an input LOW load factor of:

$$\frac{0.4 \text{ mA}}{1.6 \text{ mA}} \text{ or } 0.25 \text{ U.L.} \quad \text{an input HIGH load factor of} \quad \frac{20 \mu\text{A}}{40 \mu\text{A}} \quad \text{or } 0.5 \text{ U.L.}$$

**EXAMPLES — OUTPUT DRIVE**

1. The output of the 7400 will sink 16 mA in the LOW (logic “0”) state and source 800  $\mu$ A in the HIGH (logic “1”) state. The normalized output LOW drive factor is therefore:

$$\frac{16 \text{ mA}}{1.6 \text{ mA}} = 10 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800 \mu\text{A}}{40 \mu\text{A}} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400  $\mu$ A in the HIGH state. The normalized output LOW drive factor is:

$$\frac{8.0 \text{ mA}}{1.6 \text{ mA}} = 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400 \mu\text{A}}{40 \mu\text{A}} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 4.

**Table 4.**

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74 ALS	0.5 U.L.	0.0625 U.L.	10 U.L.	5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

## WIRED-OR APPLICATIONS

Certain TTL devices are provided with an “open” collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required  $V_{OH}$  with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

## MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \cdot 1.6 \text{ mA}}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \cdot I_{OH} + N_2(HIGH) \cdot 40 \mu\text{A}}$$

where:

$R_x$	= External Pull-up Resistor
$N_1$	= Number of Wired-OR Outputs
$N_2$	= Number of Input Unit Loads (U.L.) being Driven
$I_{OH} = I_{CEX}$	= Output HIGH Leakage Current
$I_{OL}$	= LOW Level Fan-out Current of Driving Element
$V_{OL}$	= Output LOW Voltage Level (0.5 V)
$V_{OH}$	= Output HIGH Voltage Level (2.4 V)
$V_{CC}$	= Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25 \text{ V} - 0.5 \text{ V}}{8.0 \text{ mA} - 1.6 \text{ mA}} = \frac{4.75 \text{ V}}{6.4 \text{ mA}} = 742 \Omega$$

$$R_{X(MAX)} = \frac{4.75 \text{ V} - 2.4 \text{ V}}{4 \cdot 100 \mu\text{A} + 2 \cdot 40 \mu\text{A}} = \frac{2.35 \text{ V}}{0.48 \text{ mA}} = 4.9 \text{ k}\Omega$$

where:

$N_1$	= 4
$N_2$ (HIGH)	= 4 • 0.5 U.L. = 2 U.L.
$N_2$ (LOW)	= 4 • 0.25 U.L. = 1 U.L.
$I_{OH}$	= 100 $\mu\text{A}$
$I_{OL}$	= 8.0 mA
$V_{OL}$	= 0.5 V
$V_{OH}$	= 2.4 V

Any value of pull-up resistor between 742  $\Omega$  and 4.9 k $\Omega$  can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

## UNUSED INPUTS

For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to  $V_{CC}$ , LS TTL inputs have a breakdown voltage >7.0 V and require, therefore no series resistor.
2. Connect the unused input to the output of an unused gate that is forced HIGH.

**CAUTION:** Do not connect an unused LS input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

## INPUT CAPACITANCE

As a rule of thumb, LS TTL inputs have an average capacitance of 5.0 pF for DIP packages. For an input that serves more than one internal function, each additional function adds approximately 1.5 pF.

## LINE DRIVING

Because of its superior capacitive drive characteristics, TTL logic is often used in line driving applications which require various termination techniques to maintain signal

integrity. Parameters associated with this application are listed in Table 5.

It is also often necessary to construct load lines to determine reflection waveforms in line driving applications. The input and output characteristics graphs of Section 2 (Figures 4, 7, and 8) can be very useful for this purpose.

#### OUTPUT RISE AND FALL TIMES

provide important information in determining reflection waveforms and crosstalk coefficients. Typical rise and fall times are approximately 6 ns for LS with a 50 pF load (measured 10–90%). Output rise and fall times become longer as capacitive load is increased.

#### INTERCONNECTION DELAYS

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect

on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 100  $\Omega$  to 200  $\Omega$ ), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

**Table 5.**  
**Output Characteristics for Schottky TTL Logic**

(ALL MAXIMUM RATINGS)		LS	
Characteristic	Symbol	74LSxxx	Unit
Operating Voltage Range	$V_{CC}$	$5 \pm 5\%$	Vdc
Output Drive: Standard Output	$I_{OH}$	-0.4	mA
	$I_{OL}$	8.0	mA
	$I_{SC}$	-20 to -100	mA
Buffer Output	$I_{OH}$	-15	mA
	$I_{OL}$	24	mA
	$I_{SC}$	-40 to -225	mA

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal

transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

Functional operation under these conditions is not implied.

CHARACTERISTIC	LS
Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	-0.5 V to +15 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Open Collector Outputs (Output HIGH)	-0.5 V to +10 V
High Level Voltage Applied to Disabled 3-State Output	5.5 V
Current Applied to Output in Low State (Max)	Twice Rated I <sub>OL</sub>

\*Either input voltage limit or input current limit is sufficient to protect the inputs — Circuits with 5.5 V maximum limits are listed below.

Device types having inputs limited to 5.5 V are as follows:

- SN74LS245 — Inputs connected to outputs.
- SN74LS640/641/642/645 — Inputs connected to outputs.
- SN74LS299 — Certain Inputs.
- SN74LS151/251 — Multiplexer Inputs.

## DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA BOOK

**CURRENTS** — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

$I_{CC}$	<b>Supply Current</b> — The current flowing into the $V_{CC}$ supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.
$I_{IH}$	<b>Input HIGH current</b> — The current flowing into an input when a specified HIGH voltage is applied to that input.
$I_{IL}$	<b>Input LOW current</b> — The current flowing out of an input when a specified LOW voltage is applied to that input.
$I_{OH}$	<b>Output HIGH current.</b> The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the $I_{OH}$ is the current flowing out of an output which is in the HIGH state.
$I_{OL}$	<b>Output LOW current</b> — The current flowing into an output which is in the LOW state.
$I_{OS}$	<b>Output short-circuit current</b> — The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).
$I_{OZH}$	<b>Output off current HIGH</b> — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
$I_{OZL}$	<b>Output off current LOW</b> — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

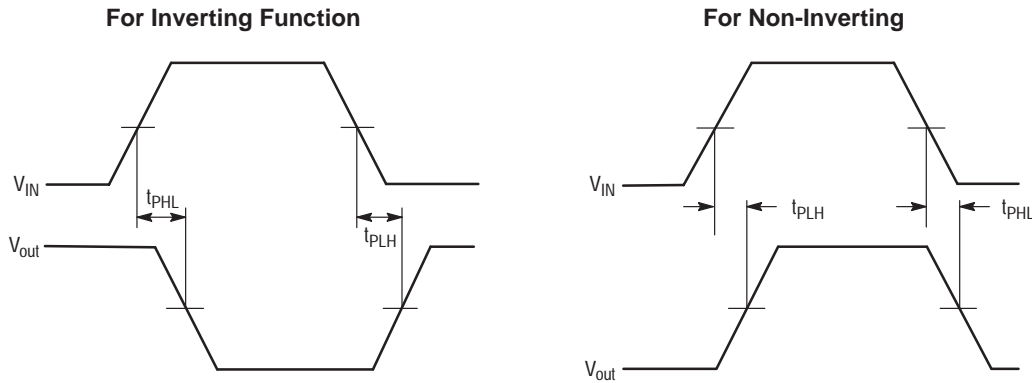
**VOLTAGES** — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*,  $-10$  V is greater than  $-1.0$  V).

$V_{CC}$	<b>Supply voltage</b> — The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
$V_{IK(MAX)}$	<b>Input clamp diode voltage</b> — The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.
$V_{IH}$	<b>Input HIGH voltage</b> — The range of input voltages recognized by the device as a logic HIGH.
$V_{IH(MIN)}$	<b>Minimum input HIGH voltage</b> — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.
$V_{IL}$	<b>Input LOW voltage</b> — The range of input voltages recognized by the device as a logic LOW.
$V_{IL(MAX)}$	<b>Maximum input LOW voltage</b> — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.
$V_{OH(MIN)}$	<b>Output HIGH voltage</b> — The minimum guaranteed voltage at an output terminal for the specified output current $I_{OH}$ and at the minimum value of $V_{CC}$ .
$V_{OL(MAX)}$	<b>Output LOW voltage</b> — The maximum guaranteed voltage at an output terminal sinking the maximum specified load current $I_{OL}$ .
$V_{T+}$	<b>Positive-going threshold voltage</b> — The input voltage of a variable threshold device ( <i>i.e.</i> , Schmitt Trigger) that is interpreted as a $V_{IH}$ as the input transition rises from below $V_{T-(MIN)}$ .
$V_{T-}$	<b>Negative-going threshold voltage</b> — The input voltage of a variable threshold device ( <i>i.e.</i> , Schmitt Trigger) that is interpreted as a $V_{IL}$ as the input transition falls from above $V_{T+(MAX)}$ .

## AC SWITCHING PARAMETERS AND WAVEFORMS

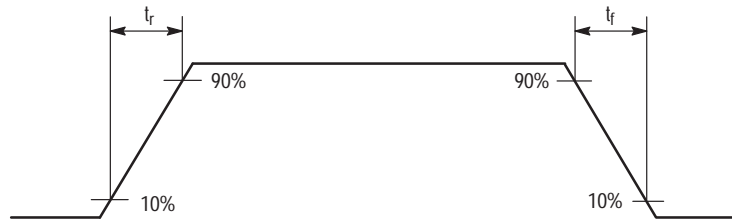
$t_{PLH}$  **LOW-TO-HIGH propagation delay time :**  
The time delay between specified reference points, typically 1.3 V for LS, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

$t_{PLH}$  **HIGH-TO-LOW propagation delay time:**  
The time delay between specified reference points, typically 1.3 V for LS, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.



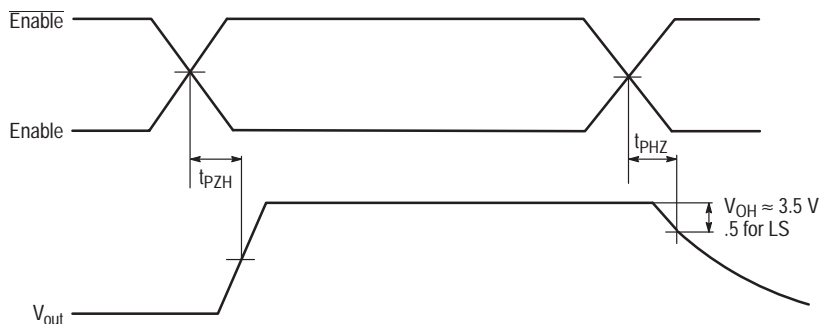
$t_r$  **Waveform Rise Time:**  
LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

$t_f$  **Waveform Fall Time:**  
HIGH to LOW logic transition time, measured the 90% to the 10% points of the waveform.



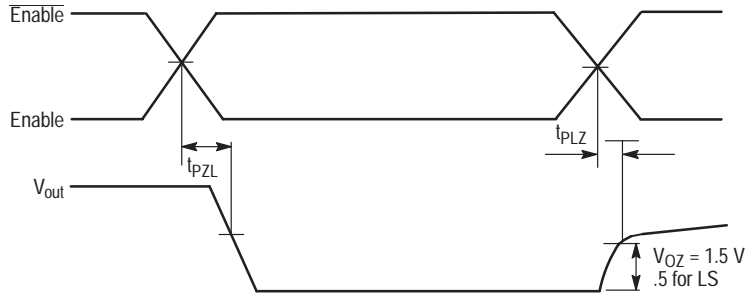
$t_{PHZ}$  **Output disable time: HIGH to Z**  
The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined HIGH level to a high impedance (OFF) state. Reference point on the output voltage waveform is  $V_{OH} - 0.5$  V for LS and  $V_{OH} - 0.3$  V for FAST.

$t_{PZH}$  **Output enable time: Z to HIGH**  
The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from a high impedance (OFF) state to a HIGH level.

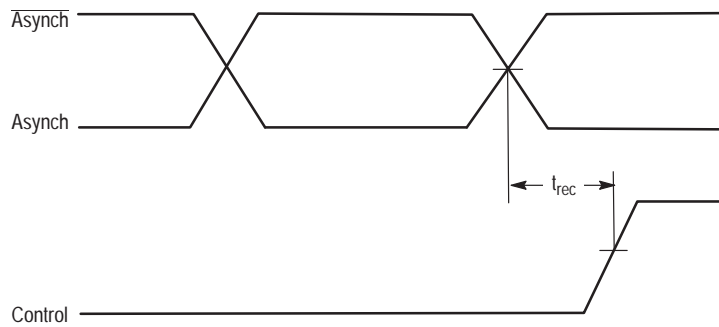


$t_{PLZ}$  **Output disable time: LOW to Z**  
 The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined LOW level to a high impedance (OFF) state. Reference point on the output voltage waveform is  $V_{OL} + 0.5\text{ V}$  for LS.

$t_{PZL}$  **Output enable time: Z to LOW**  
 The time delay between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance (OFF) state to a HIGH level.

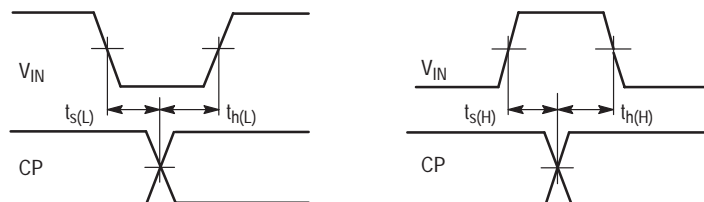


$t_{rec}$  **Recovery time**  
 Time required between an asynchronous signal (SET, RESET, CLEAR or PARALLEL load) and the active edge of a synchronous control signal, to insure that the device will properly respond to the synchronous signal.



$t_h$  **Hold Time**  
 The interval of time from the active edge of the control signal (usually the clock) to when the data to be recognized is no longer required to ensure proper interpretation of the data. A negative hold time indicates that the data may be removed at some time prior to the active edge of the control signal.

$t_s$  **Setup time**  
 The interval of time during which the data to be recognized is required to remain constant prior to the active edge of the control signal to ensure proper data recognition. A negative setup time indicates that data may be initiated sometime after the active transition of the timing pulse and still be recognized.

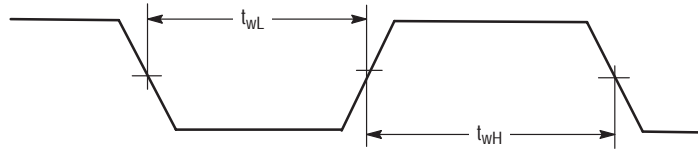




$t_w$  or  $t_{pw}$

**Pulse width**

The time between the specified amplitude points (1.3 V for LS) on the leading and trailing edges of a pulse.



$f_{MAX}$

**Toggle frequency/operating frequency**

The maximum rate at which clock pulses meeting the clock requirements (i.e.,  $t_{wH}$ ,  $t_{wL}$ , and  $t_r$ ,  $t_f$ ) may be applied to a sequential circuit. Above this frequency the device may cease to function.

$f_{MAXmin}$

**Guaranteed maximum clock frequency**

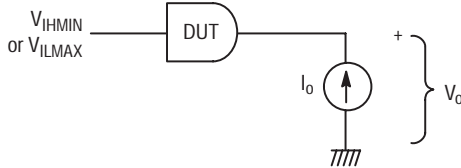
The lowest possible value for  $f_{MAX}$ .

**TESTING**

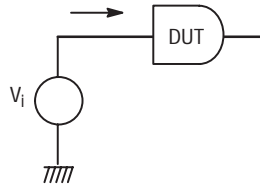
**DC TEST CIRCUITS**

The following test circuits and forcing functions represent ON Semiconductor's typical DC test procedures.

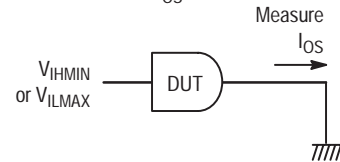
$V_{OH}$  AND  $V_{OL}$  TESTS  
Force  $I_{OHMAX}$  or  $I_{OLMAX}$   
Measure  $V_{OH}$  or  $V_{OL}$



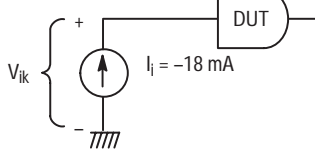
$I_{IHH}$ ,  $I_{IH}$  AND  $I_{IL}$  TESTS  
Force 7, 5.5, 2.7, or 0.4 V  
Measure  $I_{IHH}$ ,  $I_{IH}$ , or  $I_{IL}$



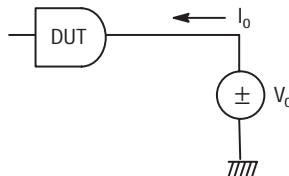
$I_{OS}$  TEST



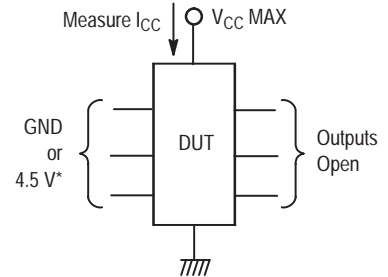
$V_{IK}$  TEST  
Force  $I_i$   
Measure  $V_{IK}$



$I_{OH}$ ,  $I_{OZH}$ , and  $I_{OZL}$  TESTS  
Force 5.5, 2.4, or 0.4 V  
Measure  $I_o$



$I_{CC}$  TEST



\*Unless otherwise indicated, input conditions are selected to produce a worst case condition.

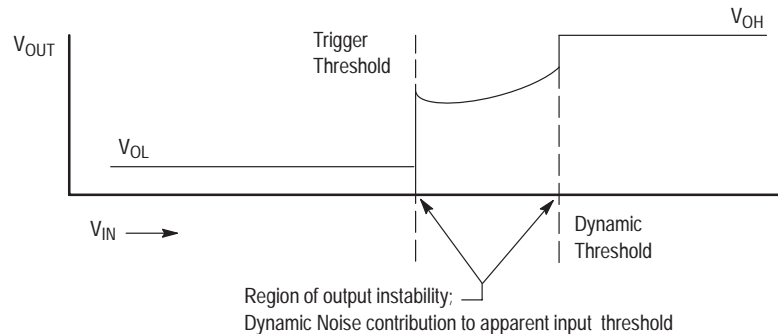
## AC TEST CIRCUITS

The following test circuits and conditions represent ON Semiconductor's typical test procedures. AC waveforms and terminology can be found on pages 22 to 24.

### FUNCTIONAL TESTING OF TTL IN A NOISY ENVIRONMENT/"DYNAMIC" THRESHOLD

Testing noise (noise generated by the test system itself and noise generated by TTL devices under test interacting with the test system) adds to, or subtracts from the threshold voltage applied to the TTL device under test. For this reason ON Semiconductor does not recommend functional testing of TTL devices using threshold levels of 0.8 V and 2.0 V.

Instead, good TTL testing techniques call for hard levels of less than 0.5 V  $V_{IL}$  and greater than 2.4 V  $V_{IH}$  to be applied for functional testing. Input threshold voltages should be tested separately, and only (for noise reasons above) after setting the device state with a hard level.



The  $V_{IN}$  versus  $V_{OUT}$  plot shows the practical effect of testing noise on a logic IC device. The actual device *Trigger threshold* is represented by the initial low to high output transition. The device will oscillate if the input voltage does not exceed the trigger threshold plus the noise generated by the interaction of the test system or given application with the device.

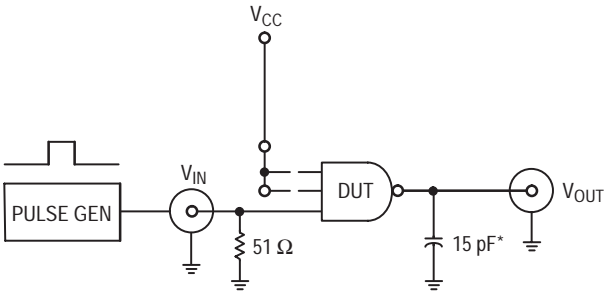
The *Dynamic threshold* (that creates Quiescent outputs), is the input logic level required to overcome the interactive DYNAMIC NOISE generated by a device switching states.

The amount of interactive DYNAMIC NOISE can be characterized by the difference between the Trigger threshold and the Dynamic threshold of the device under test. A simple number cannot be assigned to this parameter as it is heavily dependent on any given application or test environment.

So although the Trigger threshold of any given device will correlate well between any test system, the correlation of "Dynamic" threshold cannot be made directly and will have meaning only in a relative sense.

## LS TEST CIRCUITS

### Test Circuit for Standard Output Devices

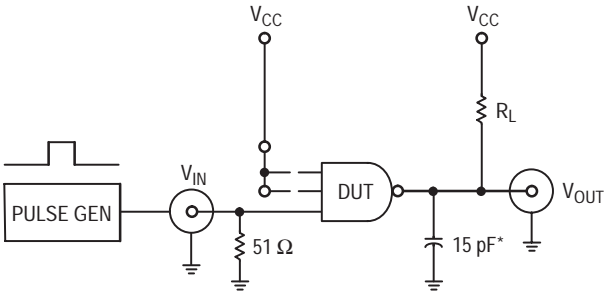


### PULSE GENERATOR SETTINGS (UNLESS OTHERWISE SPECIFIED)

LS  
 Frequency = 1 MHz  
 Duty Cycle = 50%  
 1 TLH ( $t_r$ ) = 6 ns (15)\*  
 1 THL ( $t_f$ ) = 6 ns (15)\*  
 Amplitude = 0 to 3 V

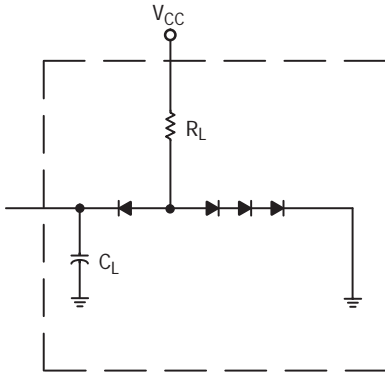
\*The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

### Test Circuit for Open Collector Output Devices



\*includes all probe and jig capacitance

### Optional LS Load (Guaranteed—Not Tested)



# APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any ON Semiconductor device listed in this catalog, please contact your local ON Semiconductor sales office or the ON Semiconductor Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting ON Semiconductor for assistance or are sending devices back to ON Semiconductor for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contains important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with ON Semiconductor representatives.

## ON Semiconductor Device Correlation/Component Analysis Request Form

— Please fill out entire form and return with devices to ON Semiconductor, R&QA Dept., 5005 E. McDowell, Phoenix, AZ 85008.

- 1) Name of Person Requesting Correlation: \_\_\_\_\_  
Phone No: \_\_\_\_\_ Job Title: \_\_\_\_\_ Company: \_\_\_\_\_
- 2) Alternate Contact: \_\_\_\_\_ Phone/Position: \_\_\_\_\_
- 3) Device Type (user part number): \_\_\_\_\_
- 4) Industry Generic Device Type: \_\_\_\_\_
- 5) # of devices tested/sampled: \_\_\_\_\_  
# of devices in question\*: \_\_\_\_\_  
# returned for correlation: \_\_\_\_\_  
\* In the event of 100% failure, does Customer have other date codes of ON Semiconductor devices that pass inspection?  
Yes \_\_\_\_\_ No \_\_\_\_\_ Please specify passing date code(s) if applicable \_\_\_\_\_  
If none, does customer have viable alternate vendor(s) for device type?  
Yes \_\_\_\_\_ No \_\_\_\_\_ Alternate vendor's name \_\_\_\_\_
- 6) Date code(s) and Serial Number(s) of devices returned for correlation — If possible, please provide one or two "good" units (ON Semiconductor's and/or other vendor) for comparison: \_\_\_\_\_
- 7) Describe USER process that device(s) are questionable in:  
\_\_\_\_\_ Incoming component inspection {test system = ?}: \_\_\_\_\_  
\_\_\_\_\_ Design prototyping: \_\_\_\_\_  
\_\_\_\_\_ Board test/burn-in: \_\_\_\_\_  
\_\_\_\_\_ Other (please describe): \_\_\_\_\_  
\_\_\_\_\_
- 8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:
  - > Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:
    - \_\_\_\_\_ Input waveform timing relationships
    - \_\_\_\_\_ Input edge rates
    - \_\_\_\_\_ Input Overshoot or Undershoot — Magnitude and Duration
    - \_\_\_\_\_ Output Overshoot or Undershoot — Magnitude and Duration
  - > Photographs, plots or sketches of relevant inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.
  - >  $V_{CC}$  and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and  $V_{CC}$  during device switching can dramatically effect input and internal operating levels. Ground &  $V_{CC}$  measurements should be made as physically close to the device in question as possible.
  - > Are there specific circumstances that seem to make the questionable unit(s) worse? Better?
    - \_\_\_\_\_ Temperature \_\_\_\_\_
    - \_\_\_\_\_  $V_{CC}$  \_\_\_\_\_
    - \_\_\_\_\_ Input rise/fall time \_\_\_\_\_
    - \_\_\_\_\_ Output loading (current/capacitance) \_\_\_\_\_
    - \_\_\_\_\_ Others \_\_\_\_\_
  - > ATE functional data should include pattern with decoding key and critical parameters such as  $V_{CC}$ , input voltages, Func step rate, voltage expected, time to measure.



## **CHAPTER 4**

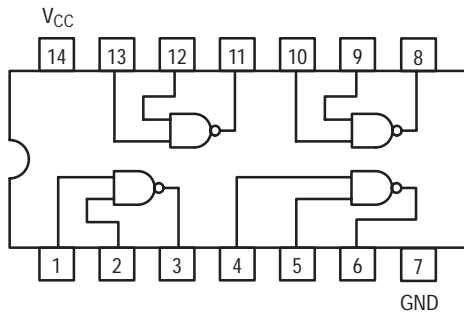
### **LS Data Sheets**

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# SN74LS00

## Quad 2-Input NAND Gate

- ESD > 3500 Volts

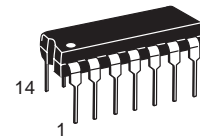


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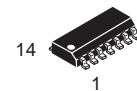
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS00N	14 Pin DIP	2000 Units/Box
SN74LS00D	14 Pin	2500/Tape & Reel

# SN74LS00

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current Total, Output HIGH			1.6	mA	$V_{CC} = \text{MAX}$
	Total, Output LOW			4.4		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

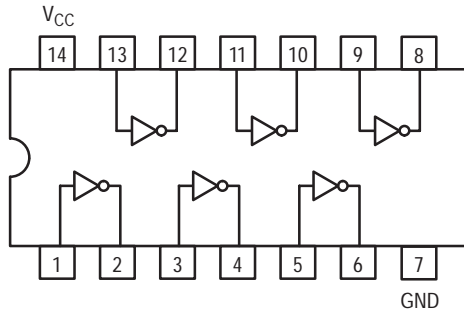
## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$	Turn-Off Delay, Input to Output		9.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PHL}$	Turn-On Delay, Input to Output		10	15	ns	



# SN74LS04

## Hex Inverter

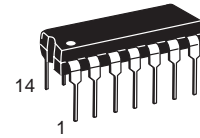


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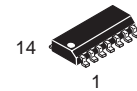
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS04N	14 Pin DIP	2000 Units/Box
SN74LS04D	14 Pin	2500/Tape & Reel

# SN74LS04

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current Total, Output HIGH			2.4	mA	$V_{CC} = \text{MAX}$
	Total, Output LOW			6.6		

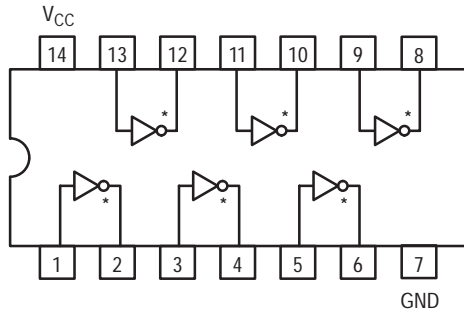
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$	Turn-Off Delay, Input to Output		9.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PHL}$	Turn-On Delay, Input to Output		10	15	ns	

# SN74LS05

## Hex Inverter



\*OPEN COLLECTOR OUTPUTS

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$V_{OH}$	Output Voltage – High			5.5	V
$I_{OL}$	Output Current – Low			8.0	mA

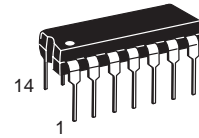


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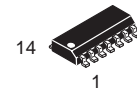
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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS05N	14 Pin DIP	2000 Units/Box
SN74LS05D	14 Pin	2500/Tape & Reel

# SN74LS05

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

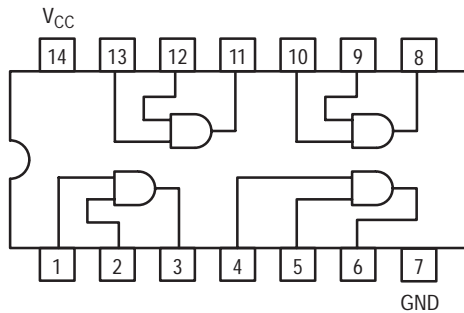
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$I_{OH}$	Output HIGH Current			100	$\mu\text{A}$	$V_{CC} = \text{MIN}$ , $V_{OH} = \text{MAX}$
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{CC}$	Power Supply Current Total, Output HIGH Total, Output LOW			2.4	mA	$V_{CC} = \text{MAX}$
				6.6		

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$	Turn-Off Delay, Input to Output		17	32	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ , $R_L = 2.0 \text{ k}\Omega$
$t_{PHL}$	Turn-On Delay, Input to Output		15	28	ns	

# SN74LS08

## Quad 2-Input AND Gate

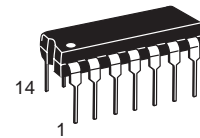


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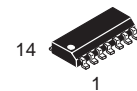
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS08N	14 Pin DIP	2000 Units/Box
SN74LS08D	14 Pin	2500/Tape & Reel

# SN74LS08

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current Total, Output HIGH			4.8	mA	$V_{CC} = \text{MAX}$
	Total, Output LOW			8.8		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$	Turn-Off Delay, Input to Output		8.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PHL}$	Turn-On Delay, Input to Output		10	20	ns	

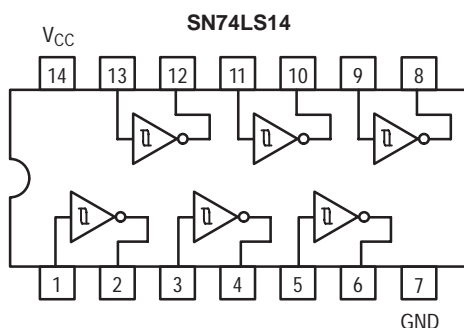
# SN74LS14

## Schmitt Triggers Dual Gate/Hex Inverter

The SN74LS14 contains logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

### LOGIC AND CONNECTION DIAGRAMS



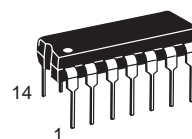
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

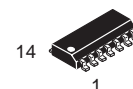


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**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 646



SOIC  
D SUFFIX  
CASE 751A

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS14N	14 Pin DIP	2000 Units/Box
SN74LS14D	14 Pin	2500/Tape & Reel

# SN74LS14

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{T+}$	Positive-Going Threshold Voltage	1.5		2.0	V	$V_{CC} = 5.0\text{ V}$
$V_{T-}$	Negative-Going Threshold Voltage	0.6		1.1	V	$V_{CC} = 5.0\text{ V}$
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V	$V_{CC} = 5.0\text{ V}$
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18\text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.4		V	$V_{CC} = \text{MIN}$ , $I_{OH} = -400\text{ }\mu\text{A}$ , $V_{IN} = V_{IL}$
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = \text{MIN}$ , $I_{OL} = 4.0\text{ mA}$ , $V_{IN} = 2.0\text{ V}$
			0.35	0.5	V	$V_{CC} = \text{MIN}$ , $I_{OL} = 8.0\text{ mA}$ , $V_{IN} = 2.0\text{ V}$
$I_{T+}$	Input Current at Positive-Going Threshold		-0.14		mA	$V_{CC} = 5.0\text{ V}$ , $V_{IN} = V_{T+}$
$I_{T-}$	Input Current at Negative-Going Threshold		-0.18		mA	$V_{CC} = 5.0\text{ V}$ , $V_{IN} = V_{T-}$
$I_{IH}$	Input HIGH Current		1.0	20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7\text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0\text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4\text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$ , $V_{OUT} = 0\text{ V}$
$I_{CC}$	Power Supply Current		8.6	16	mA	$V_{CC} = \text{MAX}$
	Total, Output HIGH					
	Total, Output LOW		12	21		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Max	Unit	Test Conditions
$t_{PLH}$	Propagation Delay, Input to Output	22	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
$t_{PHL}$	Propagation Delay, Input to Output	22	ns	

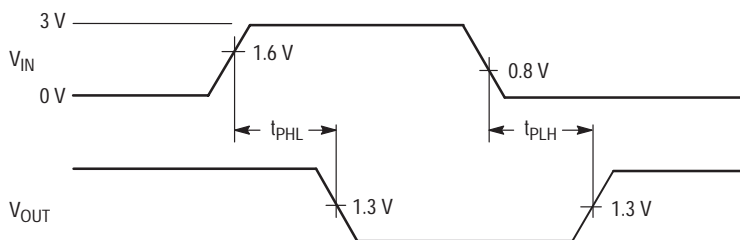


Figure 1. AC Waveforms



# SN74LS14

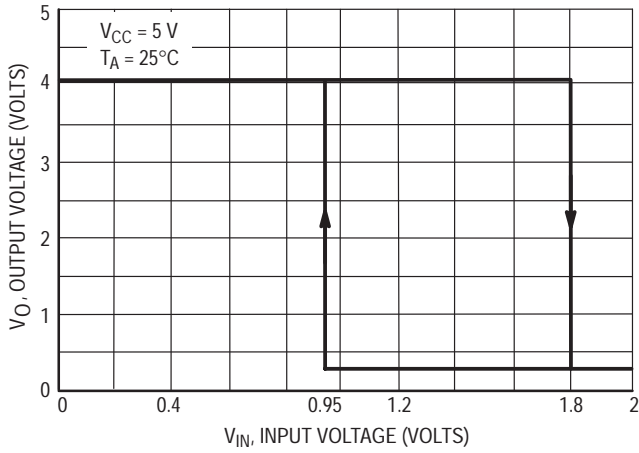


Figure 2.  $V_{IN}$  versus  $V_{OUT}$  Transfer Function

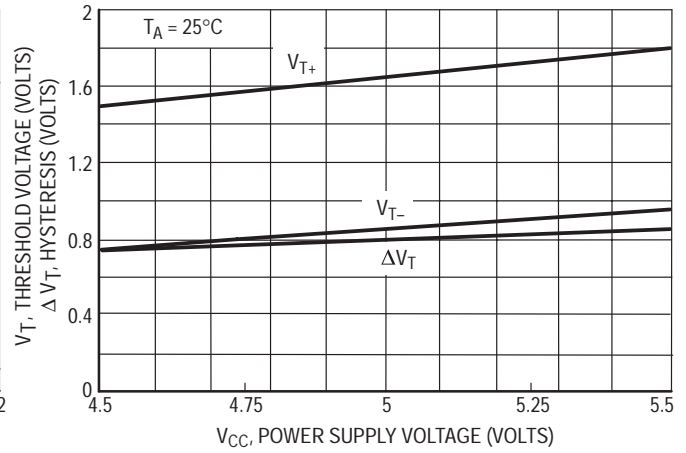


Figure 3. Threshold Voltage and Hysteresis versus Power Supply Voltage

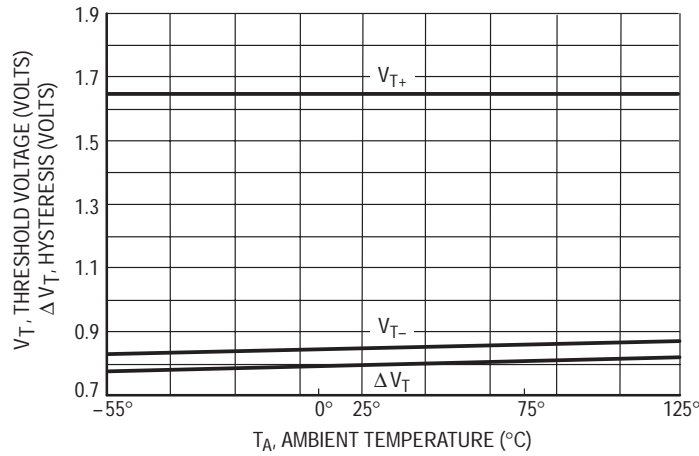
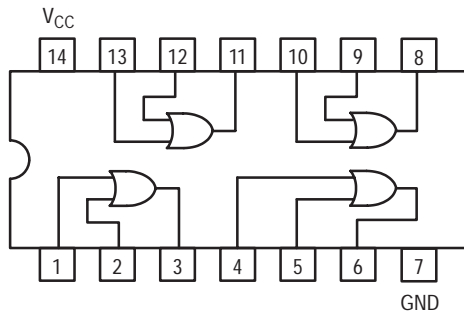


Figure 4. Threshold Voltage Hysteresis versus Temperature

# SN74LS32

## Quad 2-Input OR Gate



**ON Semiconductor**

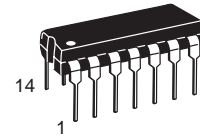
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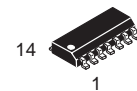
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS32N	14 Pin DIP	2000 Units/Box
SN74LS32D	14 Pin	2500/Tape & Reel

# SN74LS32

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			6.2	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			9.8		

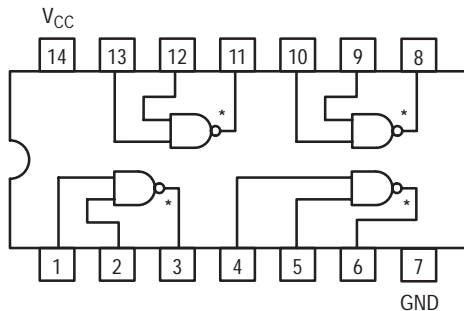
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub>	Turn-Off Delay, Input to Output		14	22	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Turn-On Delay, Input to Output		14	22	ns	

# SN74LS38

## Quad 2-Input NAND Buffer



\*OPEN COLLECTOR OUTPUTS

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$V_{OH}$	Output Voltage – High			5.5	V
$I_{OL}$	Output Current – Low			24	mA

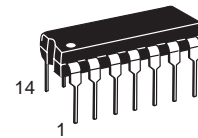


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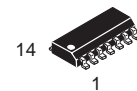
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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS38N	14 Pin DIP	2000 Units/Box
SN74LS38D	14 Pin	2500/Tape & Reel

# SN74LS38

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
I <sub>OH</sub>	Output HIGH Current			250	μA	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.4 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			2.0	mA	V <sub>CC</sub> = MAX
				12		

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>pLH</sub>	Turn-Off Delay, Input to Output		20	32	ns	V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 667 Ω C <sub>L</sub> = 45 pF
t <sub>pHL</sub>	Turn-On Delay, Input to Output		18	28	ns	

# SN74LS42

## One-of-Ten Decoder

The LSTTL/MSI SN74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Multifunction Capability
- Mutually Exclusive Outputs
- Demultiplexing Capability
- Input Clamp Diodes Limit High Speed Termination Effects

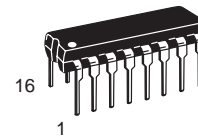
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

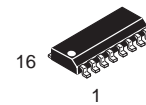


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**LOW  
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**PLASTIC  
N SUFFIX  
CASE 648**



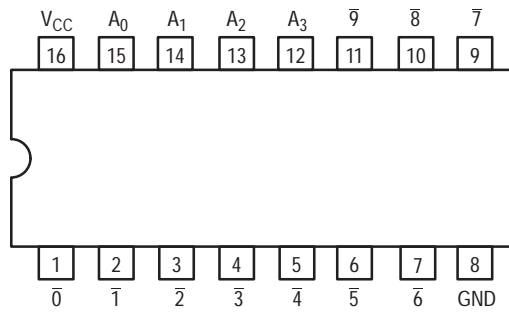
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS42N	16 Pin DIP	2000 Units/Box
SN74LS42D	16 Pin	2500/Tape & Reel

# SN74LS42

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
 The Flatpak version  
 has the same pinouts  
 (Connection Diagram)  
 as the Dual In-Line  
 Package.

### PIN NAMES

$A_0 - A_3$  Address Inputs  
 $\bar{0} - \bar{9}$  Outputs, Active LOW

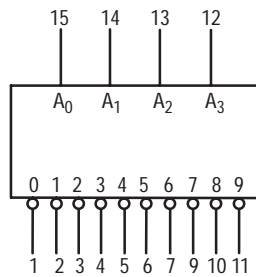
### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	5 U.L.

### NOTES:

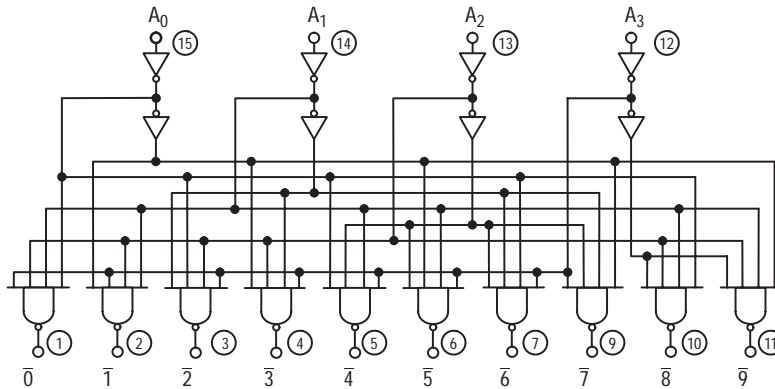
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
 GND = PIN 8

### LOGIC DIAGRAM



$V_{CC}$  = PIN 16  
 GND = PIN 8

○ = PIN NUMBERS

# SN74LS42

## FUNCTIONAL DESCRIPTION

The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input  $A_3$  produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The  $A_3$  input can also be used as the Data input in an 8-output demultiplexer application.

## TRUTH TABLE

$A_0$	$A_1$	$A_2$	$A_3$	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level



# SN74LS42

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			13	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay (2 Levels)		15 15	25 25	ns	Figure 2 $V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay (3 Levels)		20 20	30 30	ns	

## AC WAVEFORMS

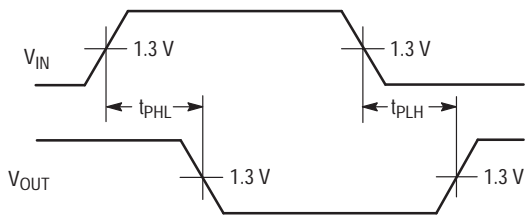


Figure 1.

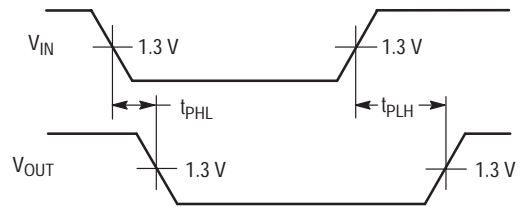


Figure 2.

# SN74LS47

## BCD to 7-Segment Decoder/Driver

The SN74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250  $\mu$ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High BI/RBO			-50	$\mu$ A
I <sub>OL</sub>	Output Current – Low BI/RBO BI/RBO			3.2	mA
V <sub>O(off)</sub>	Off-State Output Voltage a to g			15	V
I <sub>O(on)</sub>	On-State Output Current a to g			24	mA

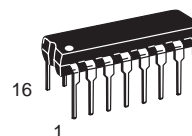


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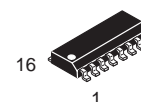
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**LOW  
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SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



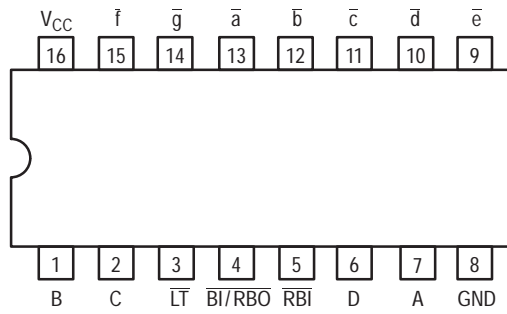
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS47N	16 Pin DIP	2000 Units/Box
SN74LS47D	16 Pin	2500/Tape & Reel

# SN74LS47

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

A, B, C, D	BCD Inputs
$\overline{RBI}$	Ripple-Blanking Input
$\overline{LT}$	Lamp-Test Input
$\overline{BI/RBO}$	Blanking Input or Ripple-Blanking Output
$\overline{a}$ , to $\overline{g}$	Outputs

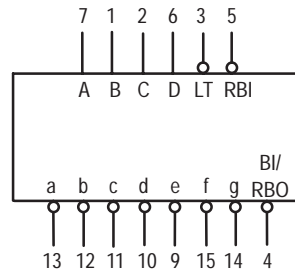
### LOADING (Note a)

	HIGH	LOW
A, B, C, D	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	0.5 U.L.	0.25 U.L.
$\overline{LT}$	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	0.5 U.L.	0.75 U.L.
$\overline{a}$ , to $\overline{g}$	1.2 U.L.	2.0 U.L.
	Open-Collector	15 U.L.

### NOTES:

- a) 1 Unit Load (U.L.) = 40  $\mu$ A HIGH, 1.6 mA LOW.
  - b) Output current measured at  $V_{OUT} = 0.5$  V
- The Output LOW drive factor is 15 U.L. for Commercial (74) Temperature Ranges.

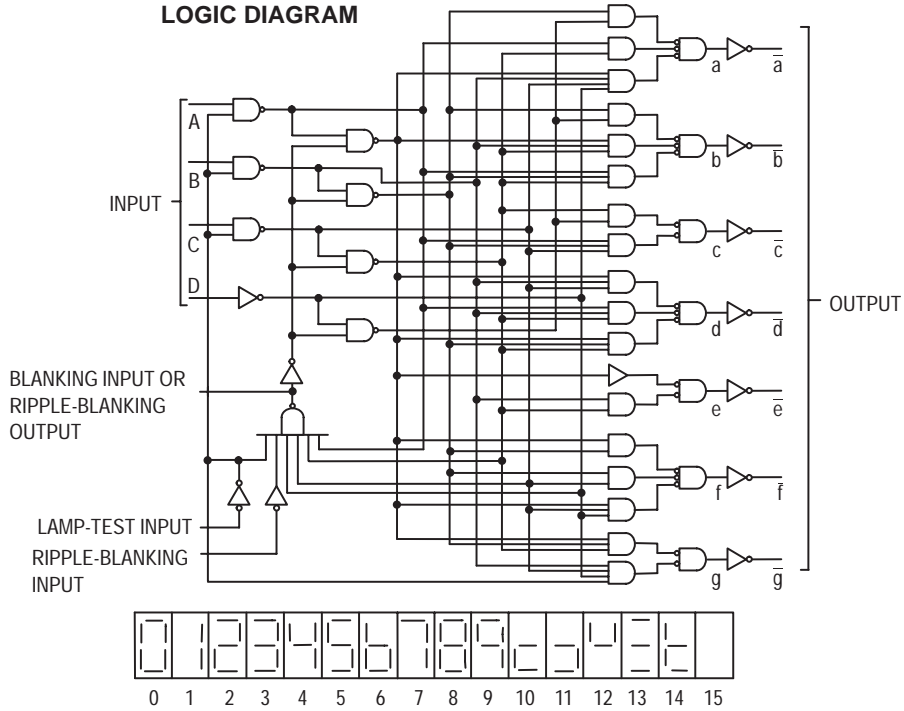
### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS47

## LOGIC DIAGRAM



## NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

## TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	LT	RBI	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

### NOTES:

- (A)  $\overline{BI/RBO}$  is wire-AND logic serving as blanking Input (BI) and/or ripple-blanking output ( $\overline{RBO}$ ). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.
- (B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.
- (C) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (D) When the blanking input/ripple-blanking output ( $\overline{BI/RBO}$ ) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

# SN74LS47

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Theshold Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage, $\overline{BI}/\overline{R\overline{B}\overline{O}}$	2.4	4.2		V	$V_{CC} = \text{MIN}$ , $I_{OH} = -50 \mu\text{A}$ , $V_{IN} = V_{IN}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage $\overline{BI}/\overline{R\overline{B}\overline{O}}$		0.25	0.4	V	$I_{OL} = 1.6 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 3.2 \text{ mA}$
$I_{O(\text{off})}$	Off-State Output Current $\overline{a}$ thru $\overline{g}$			250	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = V_{IN}$ or $V_{IL}$ per Truth Table, $V_{O(\text{off})} = 15 \text{ V}$
$V_{O(\text{on})}$	On-State Output Voltage $\overline{a}$ thru $\overline{g}$		0.25	0.4	V	$I_{O(\text{on})} = 12 \text{ mA}$
			0.35	0.5	V	$I_{O(\text{on})} = 24 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current $\overline{BI}/\overline{R\overline{B}\overline{O}}$ Any Input except $\overline{BI}/\overline{R\overline{B}\overline{O}}$			-1.2 -0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$ $\overline{BI}/\overline{R\overline{B}\overline{O}}$	Output Short Circuit Current (Note 1)	-0.3		-2.0	mA	$V_{CC} = \text{MAX}$ , $V_{OUT} = 0 \text{ V}$
$I_{CC}$	Power Supply Current		7.0	13	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PHL}$ $t_{PLH}$	Propagation Delay, Address Input to Segment Output			100	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PHL}$ $t_{PLH}$	Propagation Delay, $\overline{RB\overline{I}}$ Input To Segment Output			100	ns	
				100	ns	

## AC WAVEFORMS

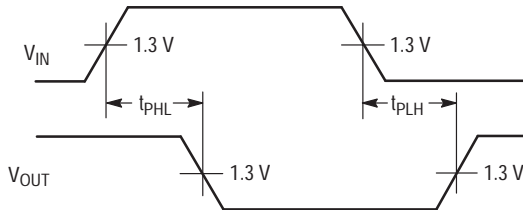


Figure 1.

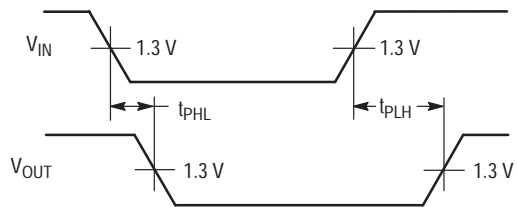


Figure 2.

# SN74LS74A

## Dual D-Type Positive Edge-Triggered Flip-Flop

The SN74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

### MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\bar{S}_D$	$\bar{C}_D$	D	Q	$\bar{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

\* Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go HIGH simultaneously. If the levels at the set and clear are near  $V_{IL}$  maximum then we cannot guarantee to meet the minimum level for  $V_{OH}$ .

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

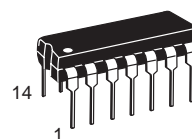
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

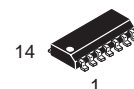


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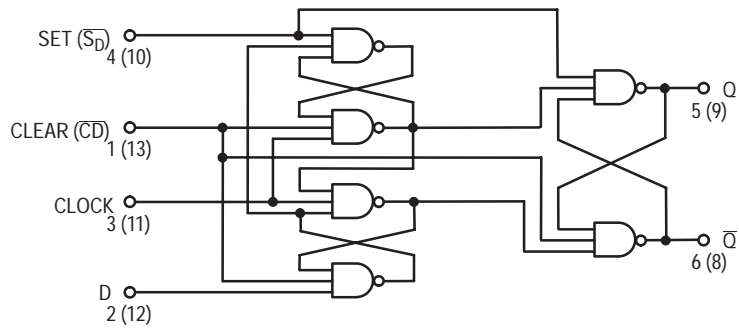
**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

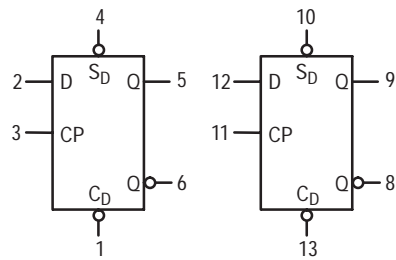
Device	Package	Shipping
SN74LS74AN	14 Pin DIP	2000 Units/Box
SN74LS74AD	14 Pin	2500/Tape & Reel

# SN74LS74A

## LOGIC DIAGRAM (Each Flip-Flop)



## LOGIC SYMBOL



$V_{CC}$  = PIN 14  
GND = PIN 7

# SN74LS74A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input High Current Data, Clock Set, Clear			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Data, Clock Set, Clear			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Data, Clock Set, Clear			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Output Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			8.0	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f <sub>MAX</sub>	Maximum Clock Frequency	25	33		MHz	Figure 1	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Clock, Clear, Set to Output		13 25	25 40	ns	Figure 1	

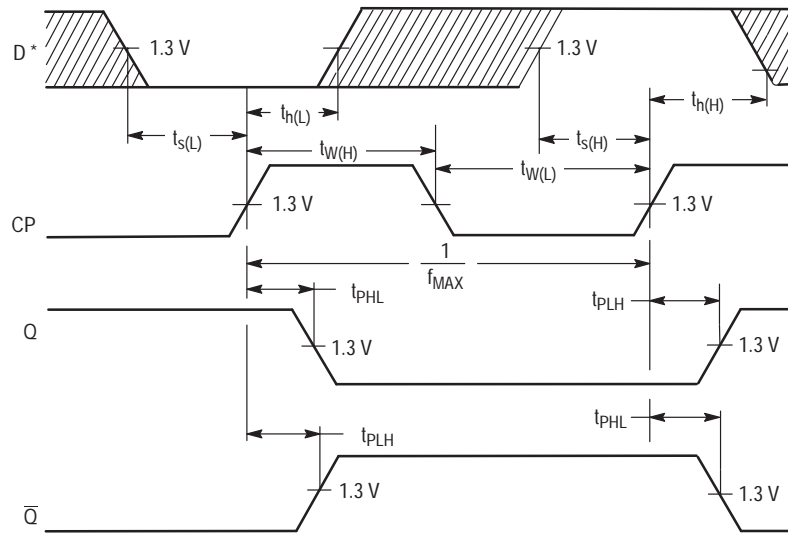
## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t <sub>W(H)</sub>	Clock	25			ns	Figure 1	V <sub>CC</sub> = 5.0 V
t <sub>W(L)</sub>	Clear, Set	25			ns	Figure 2	
t <sub>s</sub>	Data Setup Time — HIGH LOW	20			ns	Figure 1	
		20			ns		
t <sub>h</sub>	Hold Time	5.0			ns	Figure 1	



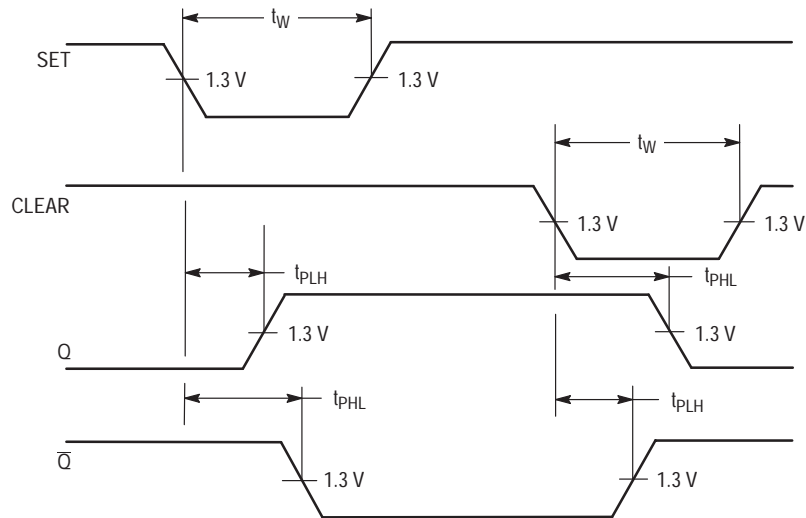
# SN74LS74A

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width**



**Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths**

# SN74LS76A

## Dual JK Flip-Flop with Set and Clear

The SN74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

### MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\bar{S}_D$	$\bar{C}_D$	J	K	Q	$\bar{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\bar{q}$

\* Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Immaterial

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH-to-LOW clock transition

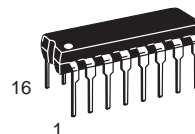
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

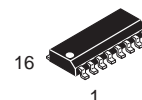


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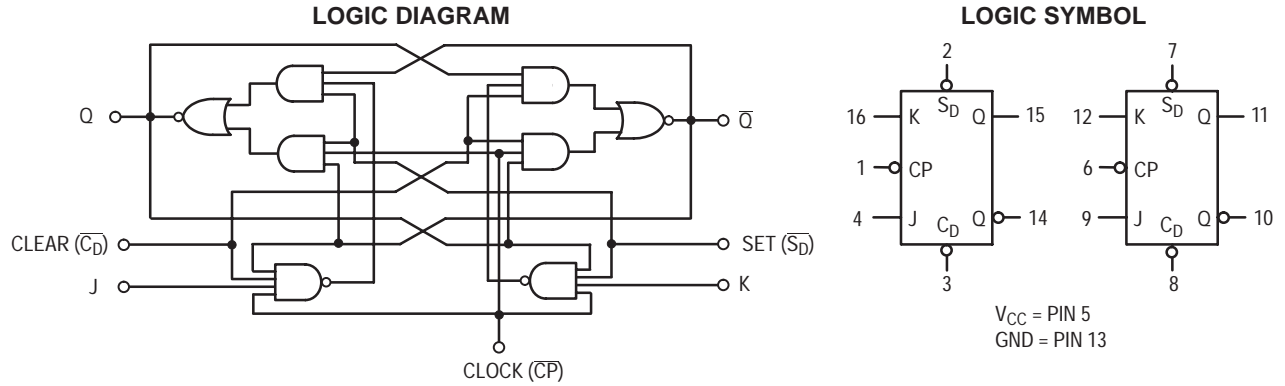


**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS76AN	16 Pin DIP	2000 Units/Box
SN74LS76AD	16 Pin	2500/Tape & Reel

# SN74LS76A



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)**

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current	J, K Clear Clock		20 60 80	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
		J, K Clear Clock		0.1 0.3 0.4	mA	
$I_{IL}$	Input LOW Current	J, K Clear, Clock		-0.4 -0.8	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)		-20	-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			6.0	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0 \text{ V}$ )**

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

**AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )**

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock Pulse Width High	20			ns	$V_{CC} = 5.0 \text{ V}$
$t_W$	Clear Set Pulse Width	25			ns	
$t_s$	Setup Time	20			ns	
$t_h$	Hold Time	0			ns	

# SN74LS85

## 4-Bit Magnitude Comparator

The SN74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ );  $A_3$ ,  $B_3$  being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: “A greater than B” ( $O_{A>B}$ ), “A less than B” ( $O_{A<B}$ ), “A equal to B” ( $O_{A=B}$ ). Three Expander Inputs,  $I_{A>B}$ ,  $I_{A<B}$ ,  $I_{A=B}$ , allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows:  $I_{A<B} = I_{A>B} = L$ ,  $I_{A=B} = H$ . For serial (ripple) expansion, the  $O_{A>B}$ ,  $O_{A<B}$  and  $O_{A=B}$  Outputs are connected respectively to the  $I_{A>B}$ ,  $I_{A<B}$ , and  $I_{A=B}$  Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$ ,  $O_{A<B}$ , and  $O_{A=B}$  Outputs Available

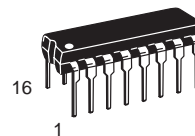
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			–0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

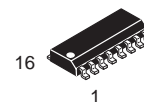


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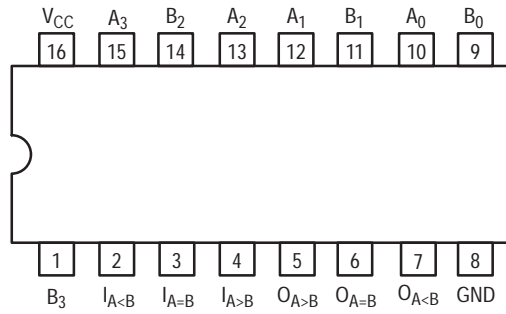
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS85N	16 Pin DIP	2000 Units/Box
SN74LS85D	16 Pin	2500/Tape & Reel

# SN74LS85

## CONNECTION DIAGRAM DIP (TOP VIEW)



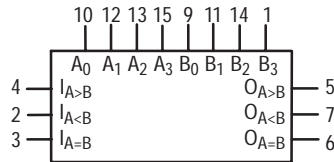
NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_3, B_0 - B_3$	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}, I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater than B Output	10 U.L.	5 U.L.
$O_{A<B}$	B Greater than A Output	10 U.L.	5 U.L.
$O_{A=B}$	A Equal to B Output	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

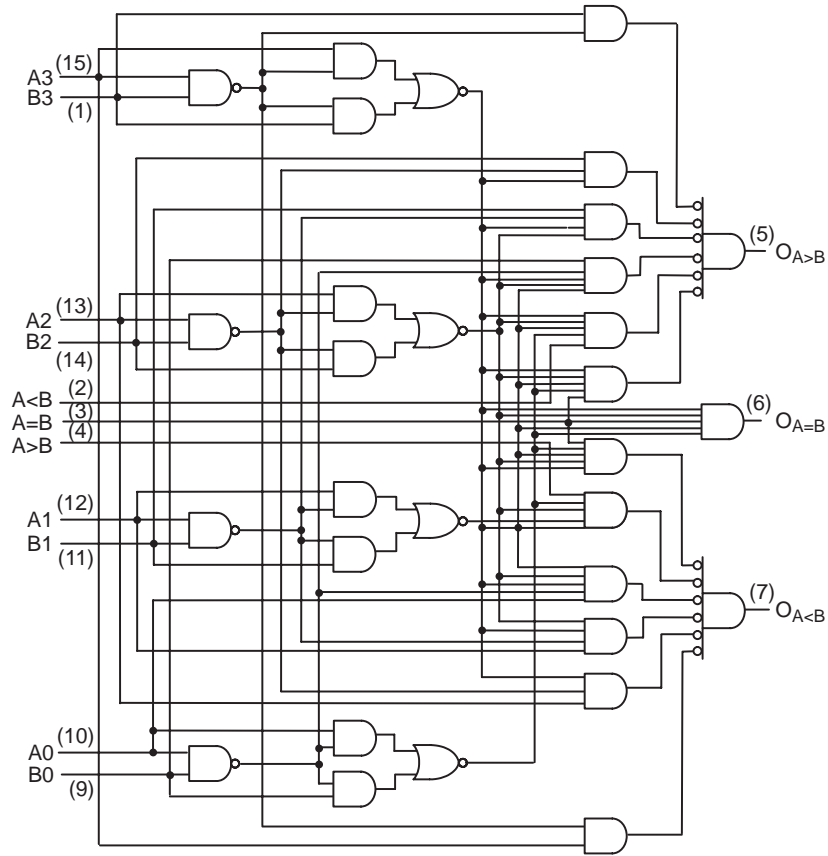
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS85

## LOGIC DIAGRAM



## TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A <sub>3</sub> ,B <sub>3</sub>	A <sub>2</sub> ,B <sub>2</sub>	A <sub>1</sub> ,B <sub>1</sub>	A <sub>0</sub> ,B <sub>0</sub>	I <sub>A&gt;B</sub>	I <sub>A&lt;B</sub>	I <sub>A=B</sub>	O <sub>A&gt;B</sub>	O <sub>A&lt;B</sub>	O <sub>A=B</sub>
A <sub>3</sub> >B <sub>3</sub>	X	X	X	X	X	X	H	L	L
A <sub>3</sub> <B <sub>3</sub>	X	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> >B <sub>2</sub>	X	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <B <sub>2</sub>	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> >B <sub>1</sub>	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> <B <sub>1</sub>	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> >B <sub>0</sub>	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> <B <sub>0</sub>	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	L	L	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	H	L	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	X	X	H	L	L	H
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	H	L	L	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	L	H	H	L

H = HIGH Level  
 L = LOW Level  
 X = IMMATERIAL

# SN74LS85

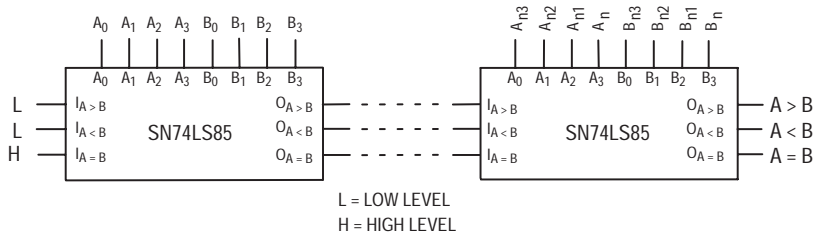


Figure 1. Comparing Two n-Bit Words

## APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result

when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:

The SN74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A<sub>0</sub>-A<sub>3</sub> and B<sub>0</sub>-B<sub>3</sub> inputs of another SN74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

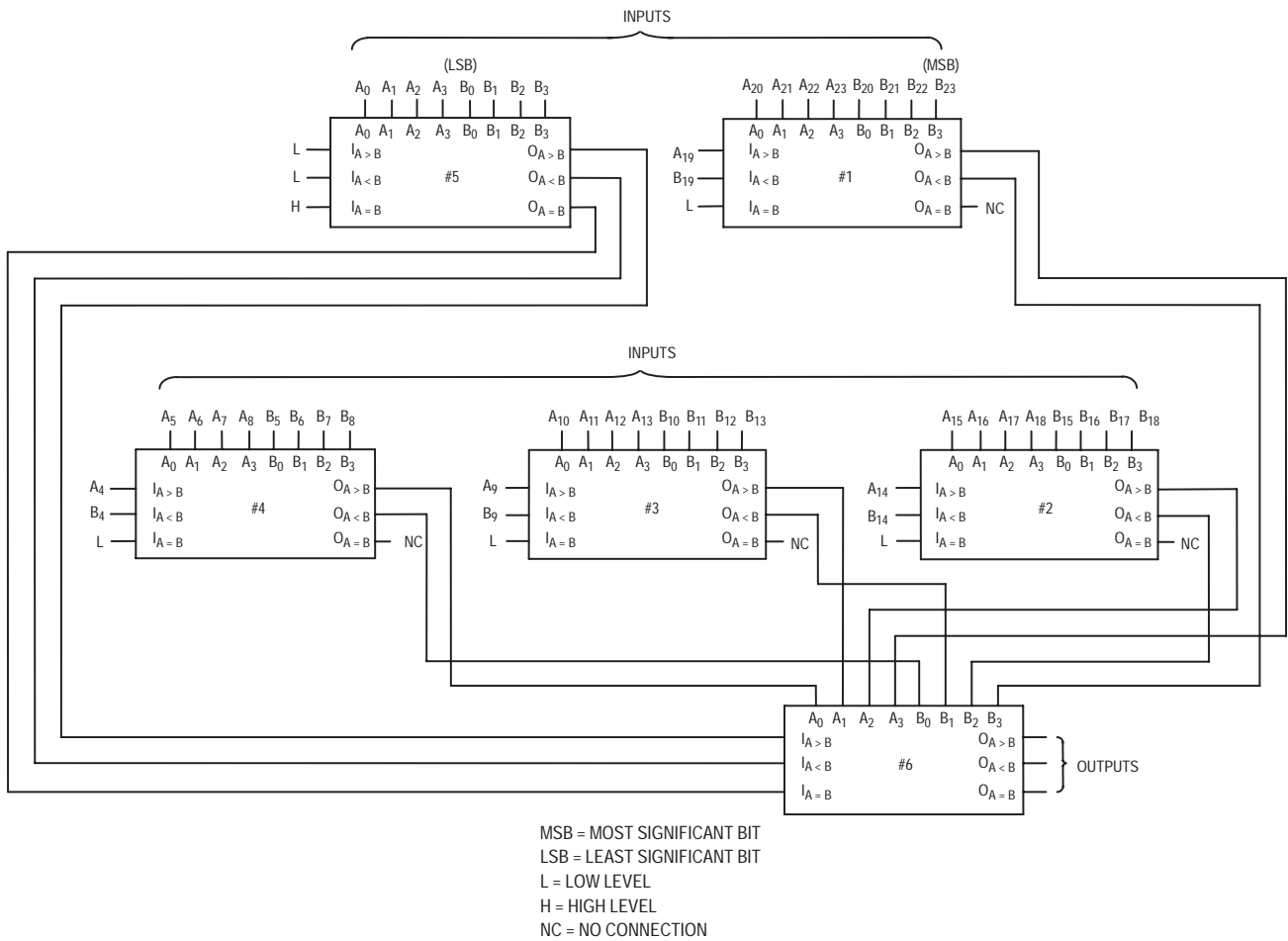


Figure 2. Comparison of Two 24-Bit Words

# SN74LS85

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current A < B, A > B Other Inputs			20 60	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
	A < B, A > B Other Inputs			0.1 0.3	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current A < B, A > B Other Inputs			-0.4 -1.2	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Output Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			20	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Any A or B to A < B, A > B		24 20	36 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Any A or B to A = B		27 23	45 45	ns	
$t_{PLH}$ $t_{PHL}$	A < B or A = B to A > B		14 11	22 17	ns	
$t_{PLH}$ $t_{PHL}$	A = B to A = B		13 13	20 26	ns	
$t_{PLH}$ $t_{PHL}$	A > B or A = B to A < B		14 11	22 17	ns	

## AC WAVEFORMS

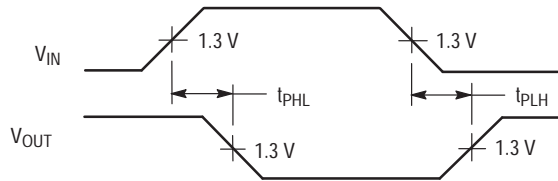


Figure 3.

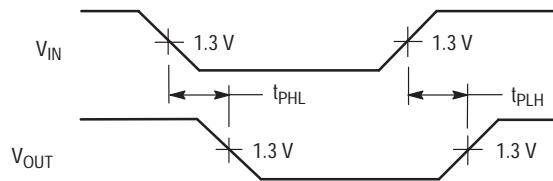
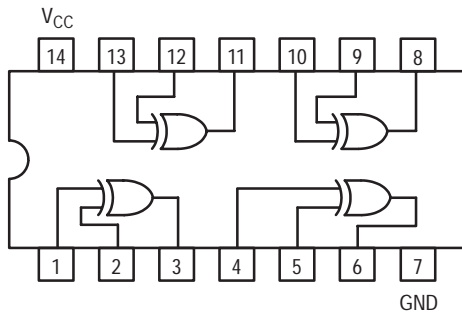


Figure 4.



# SN74LS86

## Quad 2-Input Exclusive OR Gate



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

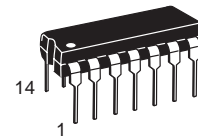
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

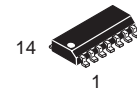


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS86N	14 Pin DIP	2000 Units/Box
SN74LS86D	14 Pin	2500/Tape & Reel

# SN74LS86

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current			40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			10	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Other Input LOW		12 10	23 17	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Other Input HIGH		20 13	30 22	ns	

# SN74LS109A

## Dual JK Positive Edge-Triggered Flip-Flop

The SN74LS109A consists of two high speed completely independent transition clocked  $\overline{JK}$  flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The  $\overline{JK}$  design allows operation as a D flip-flop by simply connecting the J and  $\overline{K}$  pins together.

### MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

\* Both outputs will be HIGH while both  $\overline{S}_D$  and  $\overline{C}_D$  are LOW, but the output states are unpredictable if  $\overline{S}_D$  and  $\overline{C}_D$  go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input

(or output) one set-up time prior to the LOW to HIGH clock transition.

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

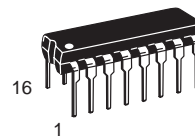


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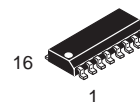
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### LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 648



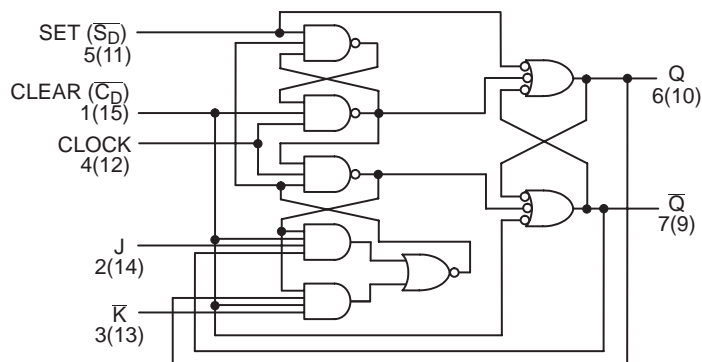
SOIC D SUFFIX CASE 751B

### ORDERING INFORMATION

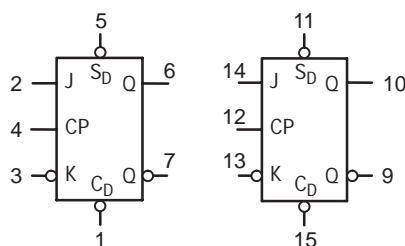
Device	Package	Shipping
SN74LS109AN	16 Pin DIP	2000 Units/Box
SN74LS109AD	16 Pin	2500/Tape & Reel

# SN74LS109A

## LOGIC DIAGRAM



## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current J, K, Clock Set, Clear			20 40	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
	J, K, Clock Set, Clear			0.1 0.2	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current J, K, Clock Set, Clear			-0.4 -0.8	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Output Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			8.0	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS109A

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Clock Frequency	25	33		MHz	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
$t_{PLH}$ $t_{PHL}$	Clock, Clear, Set to Output		13	25	ns	
			25	40	ns	

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock High Clear, Set Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
$t_s$	Data Setup Time — HIGH LOW	20			ns	
		20			ns	
$t_h$	Hold time	5.0			ns	

# SN74LS122 SN74LS123

## Retriggerable Monostable Multivibrators

These dc triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

- Overriding Clear Terminates Output Pulse
- Compensated for  $V_{CC}$  and Temperature Variations
- DC Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Internal Timing Resistors on LS122

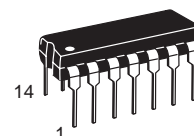
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA
$R_{ext}$	External Timing Resistance	5.0		260	k $\Omega$
$C_{ext}$	External Capacitance	No Restriction			
$R_{ext}/C_{ext}$	Wiring Capacitance at $R_{ext}/C_{ext}$ Terminal			50	pF

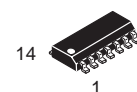


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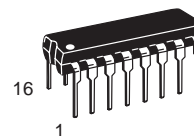
### LOW POWER SCHOTTKY



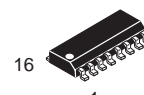
PLASTIC  
N SUFFIX  
CASE 646



SOIC  
D SUFFIX  
CASE 751A



PLASTIC  
N SUFFIX  
CASE 648



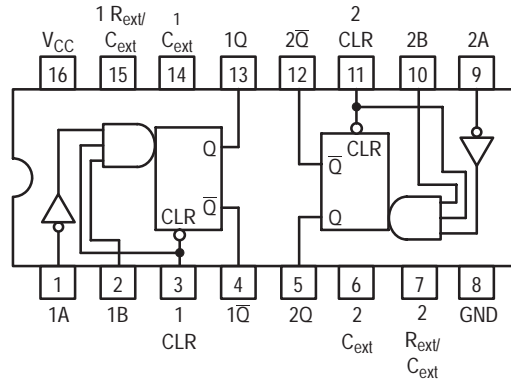
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

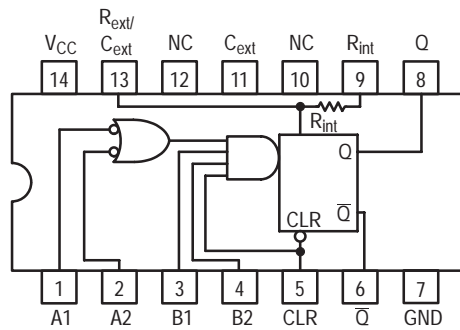
Device	Package	Shipping
SN74LS122N	14 Pin DIP	2000 Units/Box
SN74LS122D	14 Pin	2500/Tape & Reel
SN74LS123N	16 Pin DIP	2000 Units/Box
SN74LS123D	16 Pin	2500/Tape & Reel

# SN74LS122 SN74LS123

**SN74LS123 (TOP VIEW)**  
(SEE NOTES 1 THRU 4)



**SN74LS122 (TOP VIEW)**  
(SEE NOTES 1 THRU 4)



NC — NO INTERNAL CONNECTION.

**NOTES:**

1. An external timing capacitor may be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive).
2. To use the internal timing resistor of the LS122, connect  $R_{int}$  to  $V_{CC}$ .
3. For improved pulse width accuracy connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between  $R_{int}/C_{ext}$  and  $V_{CC}$ .

# SN74LS122 SN74LS123

LS122 FUNCTIONAL TABLE

INPUTS				OUTPUTS		
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H		
H	L	X	H	↑		
H	X	L	↑	H		
H	X	L	H	↑		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
↑	L	X	H	H		
↑	X	L	H	H		

LS123 FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

### TYPICAL APPLICATION DATA

The output pulse  $t_W$  is a function of the external components,  $C_{ext}$  and  $R_{ext}$  or  $C_{ext}$  and  $R_{int}$  on the LS122. For values of  $C_{ext} \geq 1000$  pF, the output pulse at  $V_{CC} = 5.0$  V and  $V_{RC} = 5.0$  V (see Figures 1, 2, and 3) is given by

$$t_W = K R_{ext} C_{ext} \text{ where } K \text{ is nominally } 0.45$$

If  $C_{ext}$  is in pF and  $R_{ext}$  is in  $k\Omega$  then  $t_W$  is in nanoseconds.

The  $C_{ext}$  terminal of the LS122 and LS123 is an internal connection to ground, however for the best system performance  $C_{ext}$  should be hard-wired to ground.

Care should be taken to keep  $R_{ext}$  and  $C_{ext}$  as close to the monostable as possible with a minimum amount of inductance between the  $R_{ext}/C_{ext}$  junction and the  $R_{ext}/C_{ext}$  pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to ensure that no false triggering occurs.

It should be noted that the  $C_{ext}$  pin is internally connected to ground on the LS122 and LS123, but not on the LS221. Therefore, if  $C_{ext}$  is hard-wired externally to ground, substitution of a LS221 onto a LS123 socket will cause the LS221 to become non-functional.

The switching diode is not needed for electrolytic capacitance application and should not be used on the LS122 and LS123.

To find the value of K for  $C_{ext} \geq 1000$  pF, refer to Figure 4. Variations on  $V_{CC}$  or  $V_{RC}$  can cause the value of K to change, as can the temperature of the LS123, LS122.

Figures 5 and 6 show the behavior of the circuit shown in Figures 1 and 2 if separate power supplies are used for  $V_{CC}$  and  $V_{RC}$ . If  $V_{CC}$  is tied to  $V_{RC}$ , Figure 7 shows how K will vary with  $V_{CC}$  and temperature. Remember, the changes in  $R_{ext}$  and  $C_{ext}$  with temperature are not calculated and included in the graph.

As long as  $C_{ext} \geq 1000$  pF and  $5K \leq R_{ext} \leq 260K$ , the change in K with respect to  $R_{ext}$  is negligible.

If  $C_{ext} \leq 1000$  pF the graph shown on Figure 8 can be used to determine the output pulse width. Figure 9 shows how K will change for  $C_{ext} \leq 1000$  pF if  $V_{CC}$  and  $V_{RC}$  are connected to the same power supply. The pulse width  $t_W$  in nanoseconds is approximated by

$$t_W = 6 + 0.05 C_{ext} (\text{pF}) + 0.45 R_{ext} (k\Omega) C_{ext} + 11.6 R_{ext}$$

In order to trim the output pulse width, it is necessary to include a variable resistor between  $V_{CC}$  and the  $R_{ext}/C_{ext}$  pin or between  $V_{CC}$  and the  $R_{ext}$  pin of the LS122. Figure 10, 11, and 12 show how this can be done.  $R_{ext}$  remote should be kept as close to the monostable as possible.

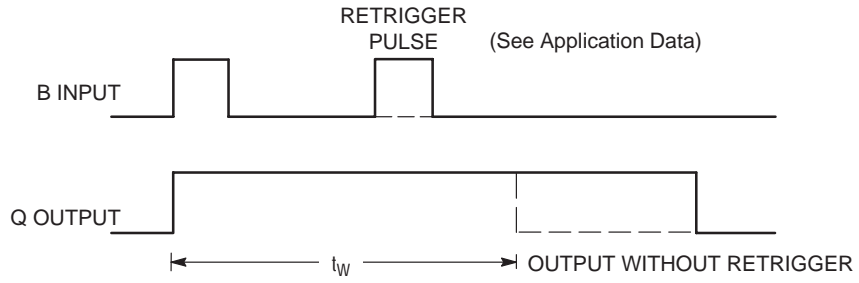
Retriggering of the part, as shown in Figure 3, must not occur before  $C_{ext}$  is discharged or the retrigger pulse will not have any effect. The discharge time of  $C_{ext}$  in nanoseconds is guaranteed to be less than  $0.22 C_{ext}$  (pF) and is typically  $0.05 C_{ext}$  (pF).

For the smallest possible deviation in output pulse widths from various devices, it is suggested that  $C_{ext}$  be kept  $\geq 1000$  pF.

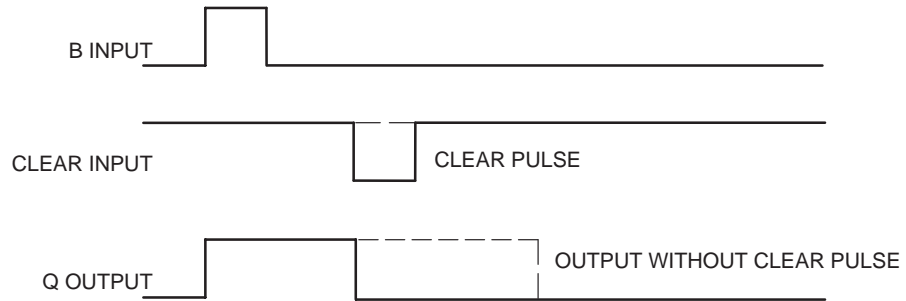


# SN74LS122 SN74LS123

## WAVEFORMS



## EXTENDING PULSE WIDTH



## OVERRIDING THE OUTPUT PULSE

# SN74LS122 SN74LS123

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current	LS122		11	mA	V <sub>CC</sub> = MAX
		LS123		20		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, A to Q Propagation Delay, A to $\bar{Q}$		23 32	33 45	ns	C <sub>ext</sub> = 0 C <sub>L</sub> = 15 pF  R <sub>ext</sub> = 5.0 kΩ R <sub>L</sub> = 2.0 kΩ
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, B to Q Propagation Delay, B to $\bar{Q}$		23 34	44 56		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clear to $\bar{Q}$ Propagation Delay, Clear to Q		28 20	45 27	ns	
t <sub>W min</sub>	A or B to Q		116	200	ns	C <sub>ext</sub> = 1000 pF, R <sub>ext</sub> = 10 kΩ, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ
t <sub>WQ</sub>	A to B to Q	4.0	4.5	5.0	μs	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Pulse Width	40			ns	

# SN74LS122 SN74LS123

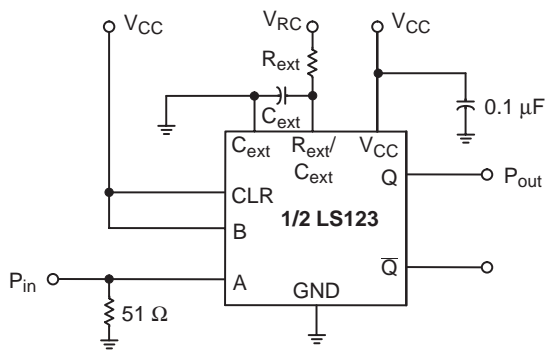


Figure 1.

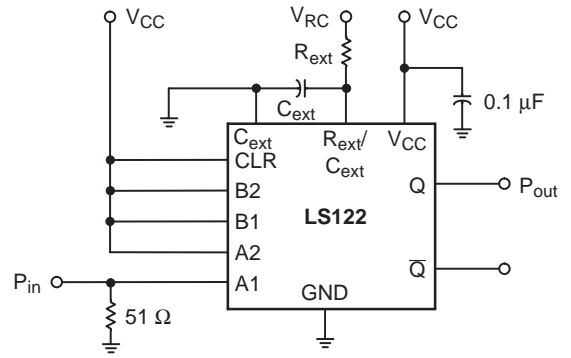


Figure 2.

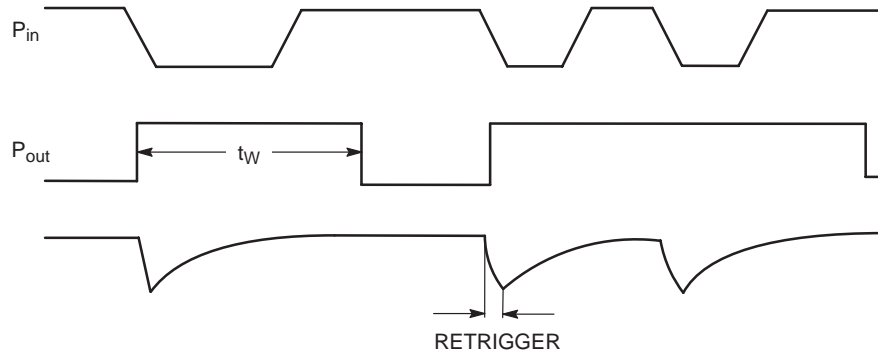


Figure 3.

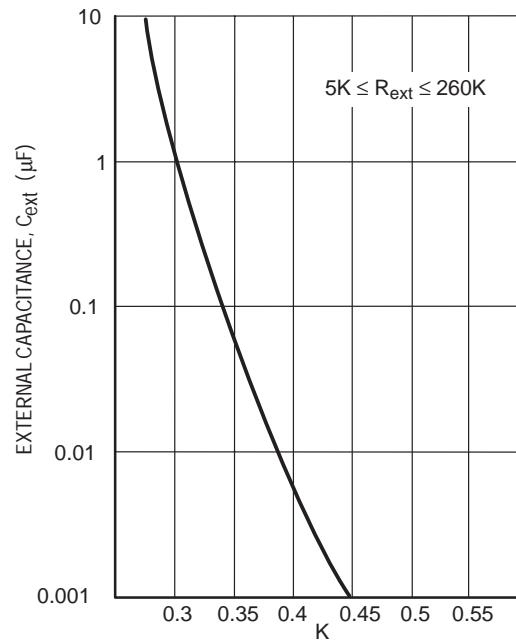


Figure 4.

# SN74LS122 SN74LS123

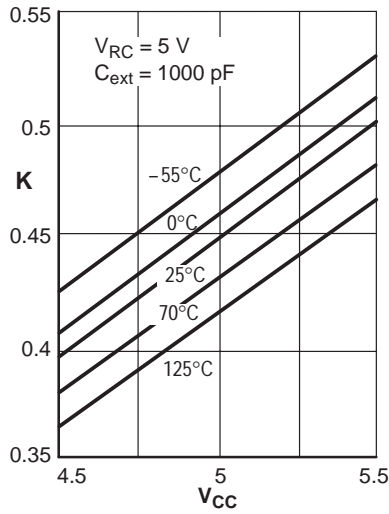


Figure 5. K versus  $V_{CC}$

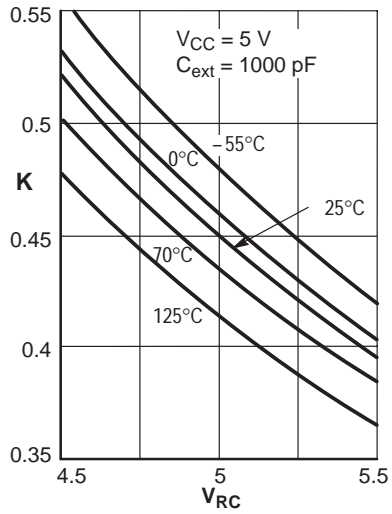


Figure 6. K versus  $V_{RC}$

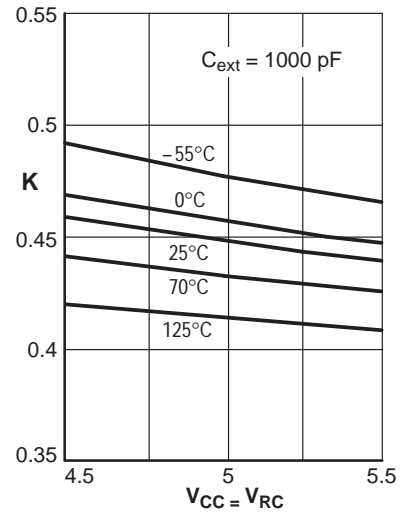


Figure 7. K versus  $V_{CC}$  and  $V_{RC}$

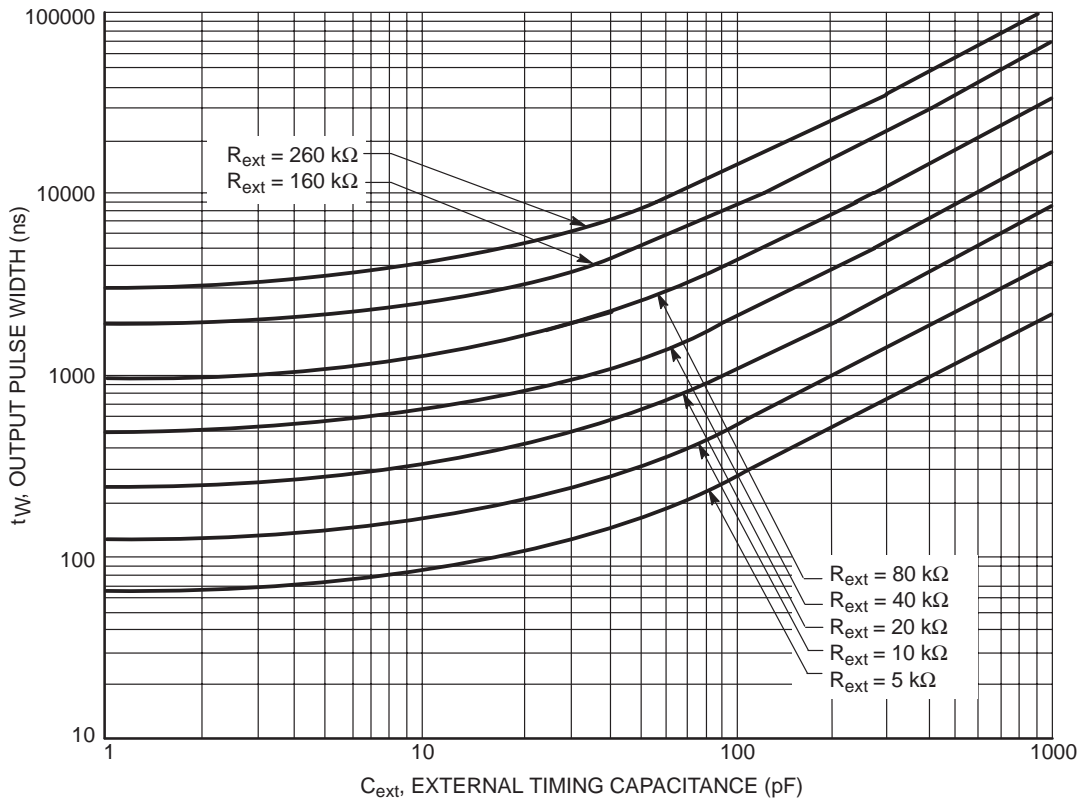


Figure 8.

# SN74LS122 SN74LS123

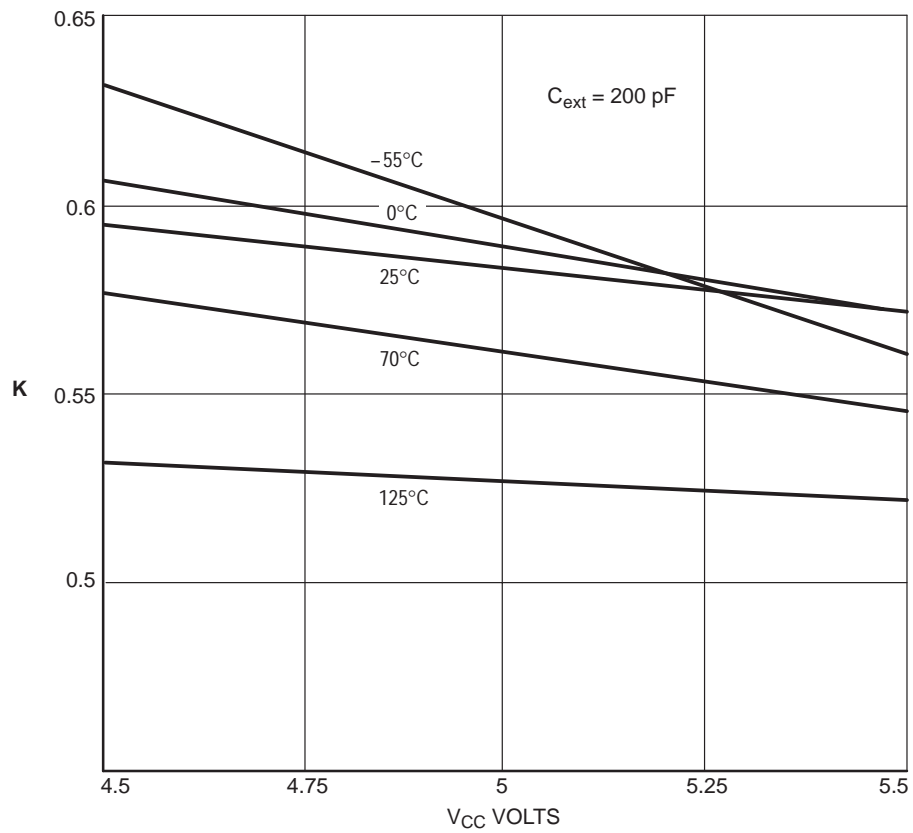


Figure 9.

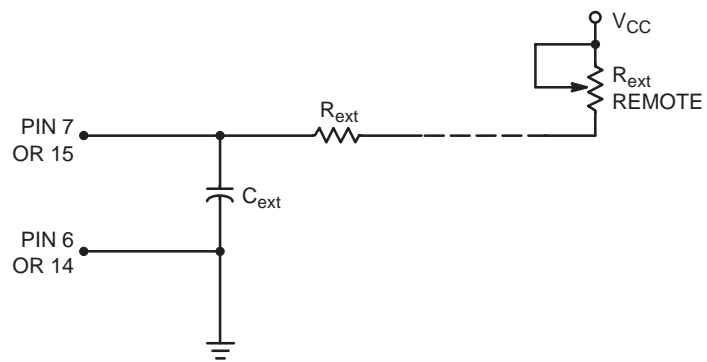


Figure 10. LS123 Remote Trimming Circuit

# SN74LS122 SN74LS123

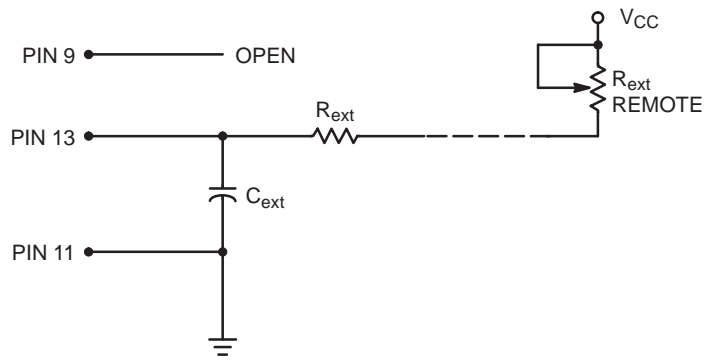


Figure 11. LS122 Remote Trimming Circuit Without  $R_{ext}$

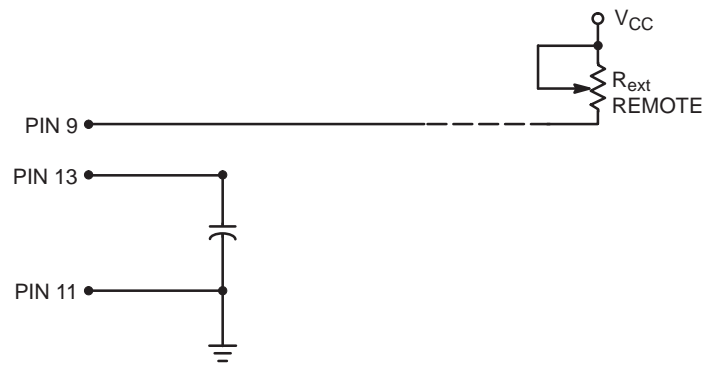


Figure 12. LS122 Remote Trimming Circuit with  $R_{int}$

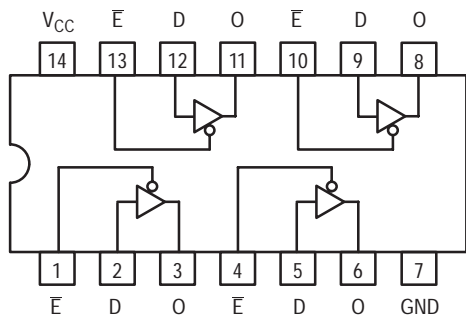
# SN74LS125A SN74LS126A

## Quad 3-State Buffers

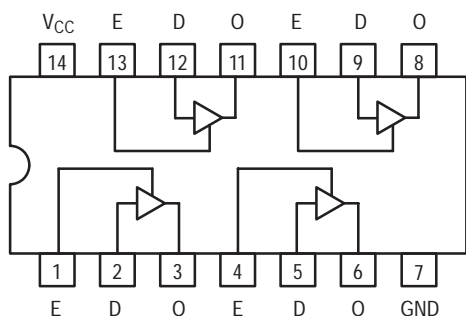


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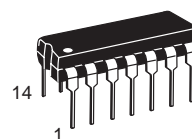
**LOW  
POWER  
SCHOTTKY**



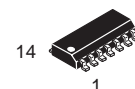
**LS125A**



**LS126A**



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### TRUTH TABLES

**LS125A**

INPUTS		OUTPUT
E	D	
L	L	L
L	H	H
H	X	(Z)

**LS126A**

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Don't Care  
(Z) = High Impedance (off)

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-2.6	mA
I <sub>OL</sub>	Output Current – Low			24	mA

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS125AN	14 Pin DIP	2000 Units/Box
SN74LS125AD	14 Pin	2500/Tape & Reel
SN74LS126AN	14 Pin DIP	2000 Units/Box
SN74LS126AD	14 Pin	2500/Tape & Reel

# SN74LS125A SN74LS126A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.4 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current	LS125A		20	mA	V <sub>CC</sub> = MAX V <sub>IN</sub> = 0 V, V <sub>E</sub> = 4.5 V
		LS126A		22		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t <sub>PLH</sub>	Propagation Delay, Data to Output	LS125A		9.0	15	ns	Figure 2  V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PLH</sub>		LS126A		9.0	15		
t <sub>PHL</sub>		LS125A		7.0	18		
t <sub>PHL</sub>		LS126A		8.0	18		
t <sub>PZH</sub>	Output Enable Time to HIGH Level	LS125A		12	20	ns	Figures 4, 5
		LS126A		16	25		
t <sub>PZL</sub>	Output Enable Time to LOW Level	LS125A		15	25	ns	Figures 3, 5
		LS126A		21	35		
t <sub>PHZ</sub>	Output Disable Time from HIGH Level	LS125A			20	ns	Figures 4, 5  V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 5.0 pF R <sub>L</sub> = 667 Ω
		LS126A			25		
t <sub>PLZ</sub>	Output Disable Time from LOW Level	LS125A			20	ns	Figures 3, 5
		LS126A			25		



# SN74LS125A SN74LS126A

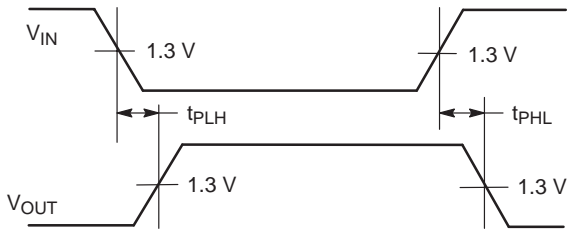


Figure 1.

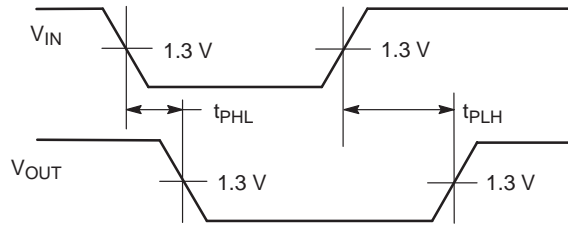


Figure 2.

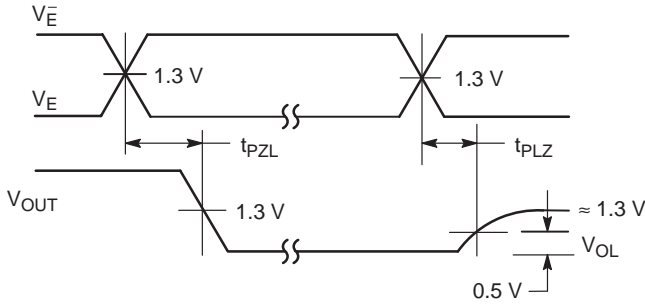


Figure 3.

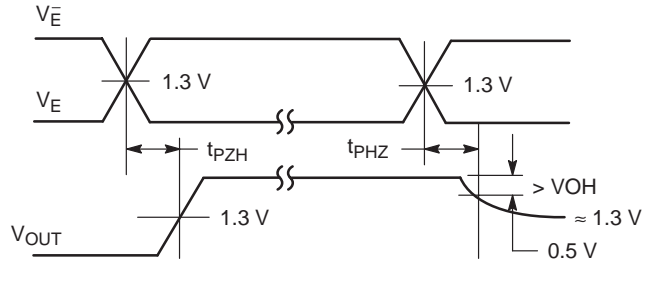


Figure 4.

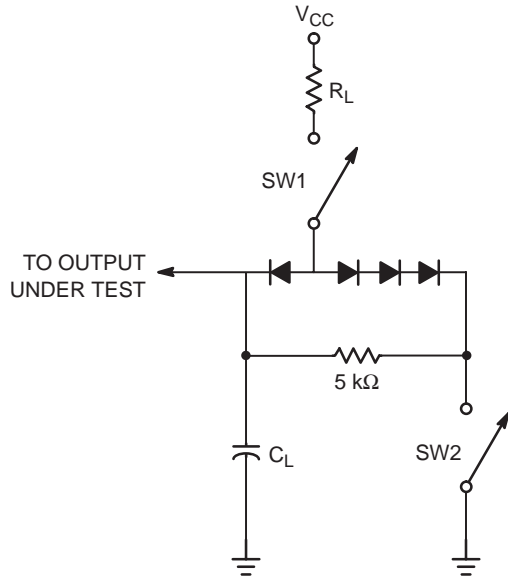


Figure 5.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

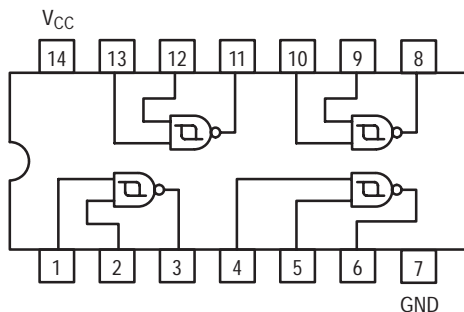
# SN74LS132

## Quad 2-Input Schmitt Trigger NAND Gate

The SN74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

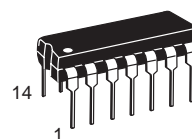
Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than  $V_{T+}$  (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

**LOGIC AND CONNECTION DIAGRAM  
DIP (TOP VIEW)**

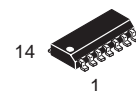


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SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS132N	14 Pin DIP	2000 Units/Box
SN74LS132D	14 Pin	2500/Tape & Reel

# SN74LS132

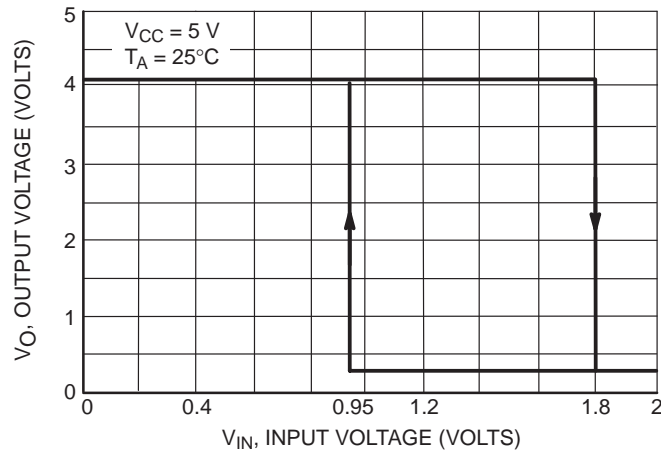


Figure 1.  $V_{IN}$  versus  $V_{OUT}$  Transfer Function

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{T+}$	Positive-Going Threshold Voltage	1.5		2.0	V	$V_{CC} = 5.0$ V
$V_{T-}$	Negative-Going Threshold Voltage	0.6		1.1	V	$V_{CC} = 5.0$ V
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V	$V_{CC} = 5.0$ V
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18$ mA
$V_{OH}$	Output HIGH Voltage	2.7	3.4		V	$V_{CC} = \text{MIN}$ , $I_{OH} = -400$ $\mu$ A, $V_{IN} = V_{IL}$
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = \text{MIN}$ , $I_{OL} = 4.0$ mA, $V_{IN} = 2.0$ V
			0.35	0.5	V	$V_{CC} = \text{MIN}$ , $I_{OL} = 8.0$ mA, $V_{IN} = 2.0$ V
$I_{T+}$	Input Current at Positive-Going Threshold		-0.14		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T+}$
$I_{T-}$	Input Current at Negative-Going Threshold		-0.18		mA	$V_{CC} = 5.0$ V, $V_{IN} = V_{T-}$
$I_{IH}$	Input HIGH Current			20	$\mu$ A	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7$ V
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0$ V
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4$ V
$I_{OS}$	Output Short Circuit Current <sup>(1)</sup>	-20		-100	mA	$V_{CC} = \text{MAX}$ , $V_{OUT} = 0$ V
$I_{CC}$	Power Supply Current Total, Output HIGH		5.9	11	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0$ V
	Total, Output LOW		8.2	14	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 4.5$ V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$	Turn-Off Delay, Input to Output			22	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF
$t_{PHL}$	Turn-On Delay, Input to Output			22	ns	

# SN74LS132

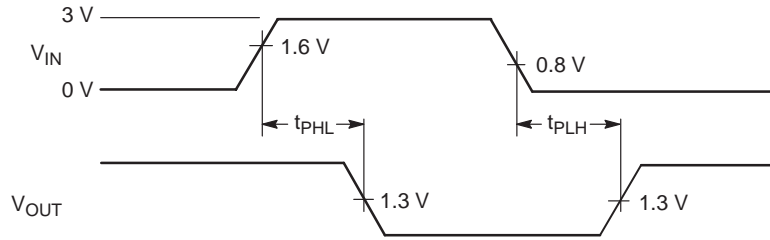


Figure 2. AC Waveforms

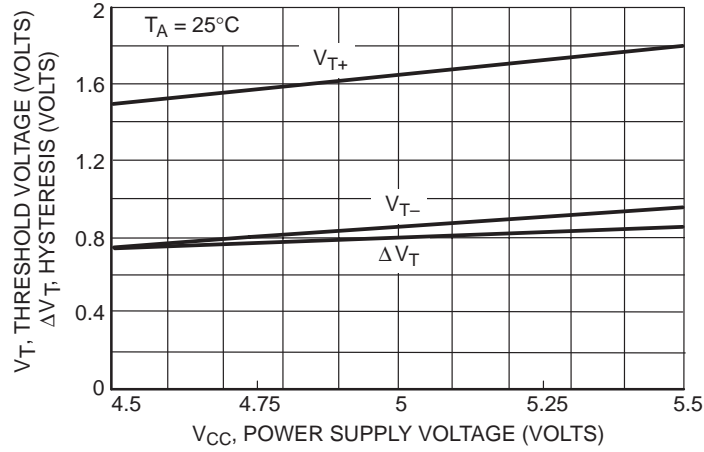


Figure 3. Threshold Voltage and Hysteresis versus Power Supply Voltage

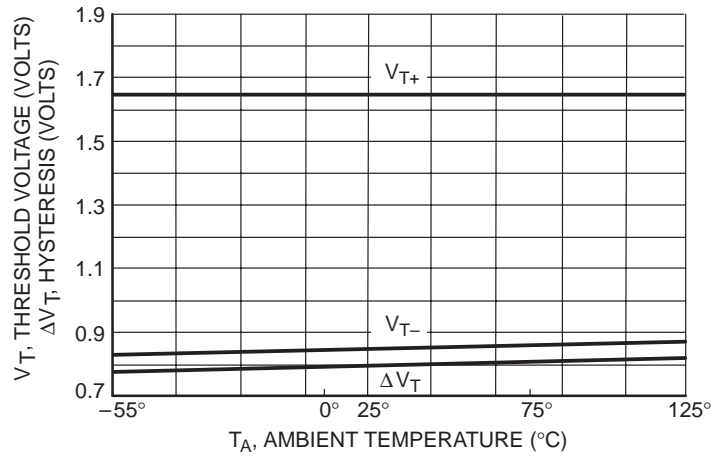


Figure 4. Threshold Voltage and Hysteresis versus Temperature

# SN74LS138

## 1-of-8 Decoder/ Demultiplexer

The LSTTL/MSI SN74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

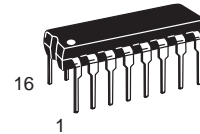
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

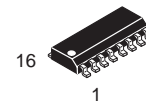


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



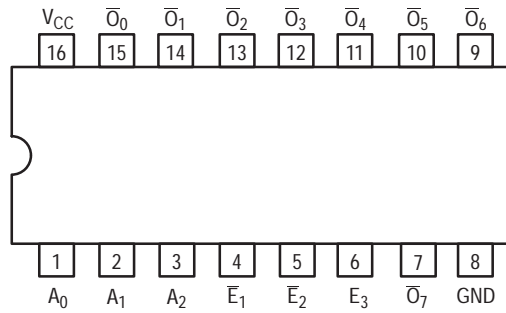
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS138N	16 Pin DIP	2000 Units/Box
SN74LS138D	16 Pin	2500/Tape & Reel

# SN74LS138

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$A_0 - A_2$	Address Inputs
$\bar{E}_1, \bar{E}_2$	Enable (Active LOW) Inputs
$E_3$	Enable (Active HIGH) Input
$\bar{O}_0 - \bar{O}_7$	Active LOW Outputs

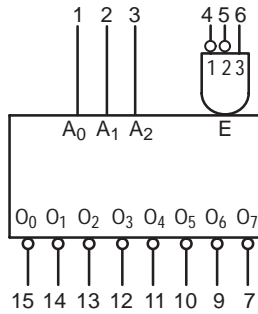
### LOADING (Note a)

	HIGH	LOW
$A_0 - A_2$	0.5 U.L.	0.25 U.L.
$\bar{E}_1, \bar{E}_2$	0.5 U.L.	0.25 U.L.
$E_3$	0.5 U.L.	0.25 U.L.
$\bar{O}_0 - \bar{O}_7$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

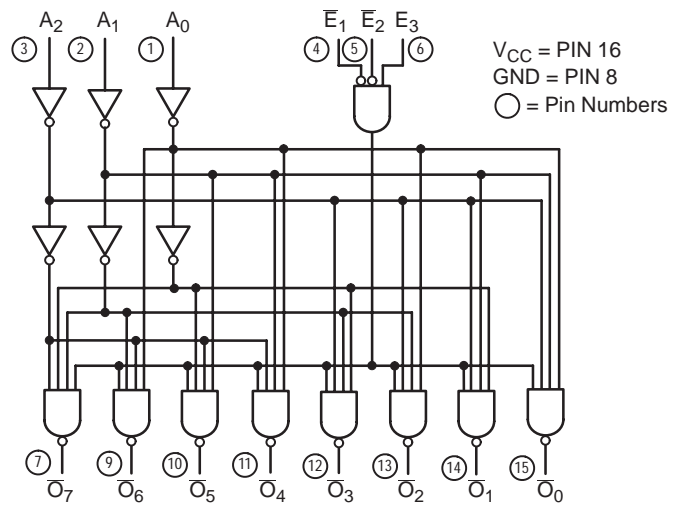
### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS138

## LOGIC DIAGRAM



# SN74LS138

## FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs ( $A_0, A_1, A_2$ ) and when enabled provides eight mutually exclusive active LOW Outputs ( $\bar{O}_0-\bar{O}_7$ ). The LS138 features three Enable inputs, two active LOW ( $\bar{E}_1, \bar{E}_2$ ) and one active HIGH ( $E_3$ ). All outputs will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH. This multiple enable

function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

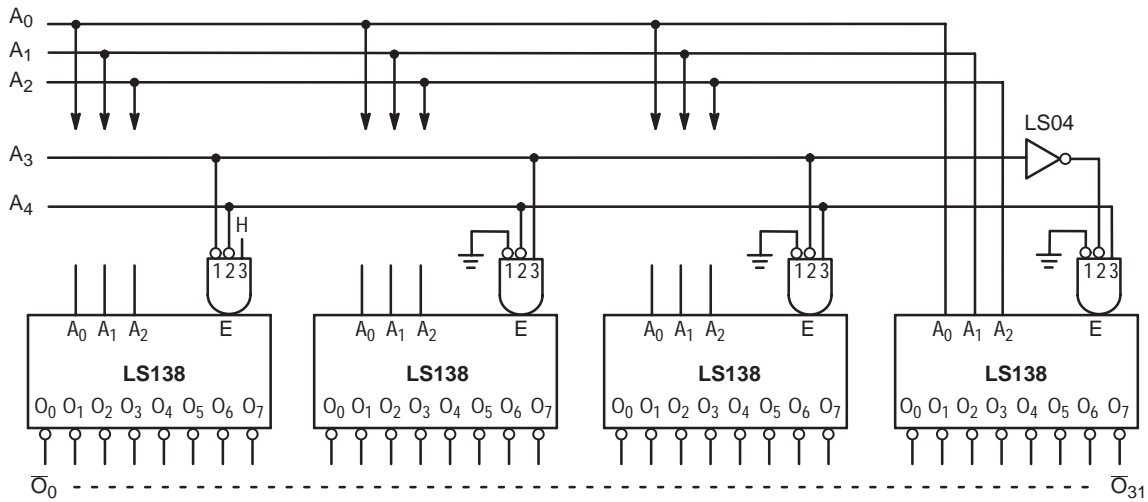


Figure a



# SN74LS138

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address to Output	2 2		13 27	20 41	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address to Output	3 3		18 26	27 39	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_1$ or $E_2$ Enable to Output	2 2		12 21	18 32	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_3$ Enable to Output	3 3		17 25	26 38	ns	

## AC WAVEFORMS

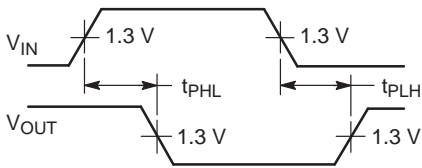


Figure 1.

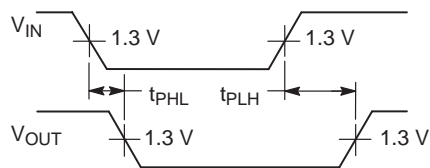


Figure 2.

# SN74LS139

## Dual 1-of-4 Decoder/ Demultiplexer

The LSTTL/MSI SN74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

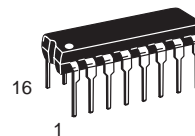
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

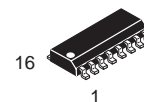


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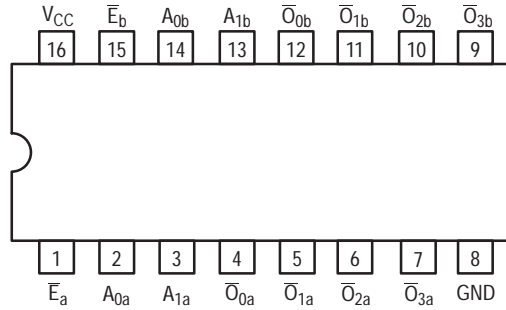
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS139N	16 Pin DIP	2000 Units/Box
SN74LS139D	16 Pin	2500/Tape & Reel

# SN74LS139

## CONNECTION DIAGRAM DIP (TOP VIEW)



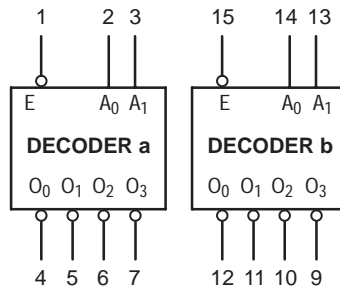
NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES	LOADING (Note a)	
	HIGH	LOW
$A_0, A_1$ Address Inputs	0.5 U.L.	0.25 U.L.
$E$ Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\bar{O}_0 - \bar{O}_3$ Active LOW Outputs	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

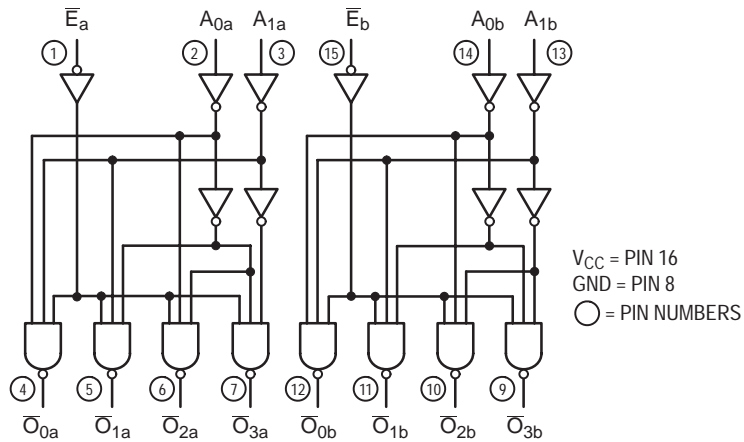
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS139

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs ( $A_0$ ,  $A_1$ ) and provide four mutually exclusive active LOW outputs ( $\bar{O}_0$ – $\bar{O}_3$ ). Each decoder has an active LOW Enable ( $\bar{E}$ ). When E is HIGH all outputs are forced HIGH. The enable

can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

### TRUTH TABLE

INPUTS			OUTPUTS			
$\bar{E}$	$A_0$	$A_1$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

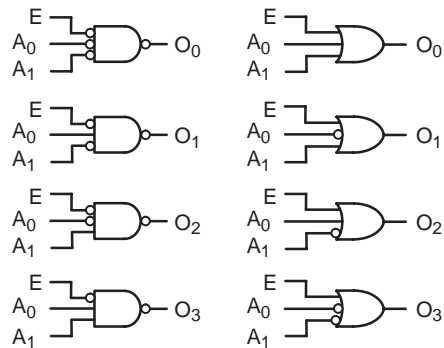


Figure a

# SN74LS139

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			11	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address to Output	2		13 22	20 33	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address to Output	3		18 25	29 38	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	2 2		16 21	24 32	ns	

## AC WAVEFORMS

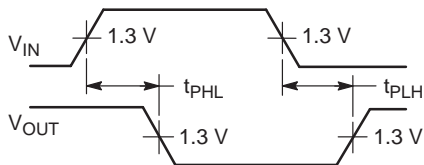


Figure 1.

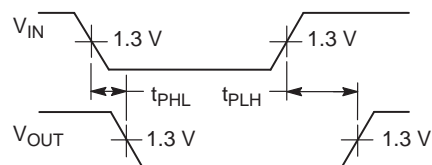


Figure 2.

# SN74LS145

## 1-of-10 Decoder/Driver Open-Collector

The SN74LS145, 1-of-10 Decoder/Driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families.

- Low Power Version of 74145
- Input Clamp Diodes Limit High Speed Termination Effects

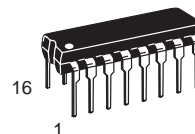
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
V <sub>OH</sub>	Output Voltage – High			15	V
I <sub>OL</sub>	Output Current – Low			24	mA

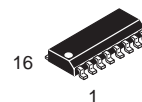


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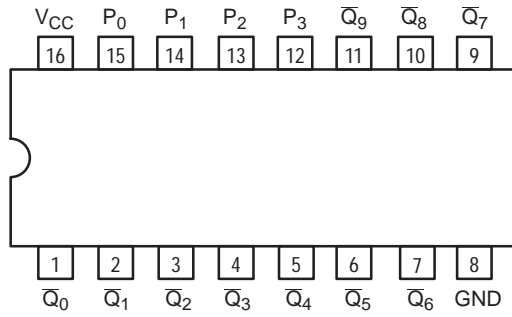
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS145N	16 Pin DIP	2000 Units/Box
SN74LS145D	16 Pin	2500/Tape & Reel

# SN74LS145

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

$P_0, P_1, P_2, P_3$  BCD Inputs  
 $\bar{Q}_0 - \bar{Q}_9$  Outputs

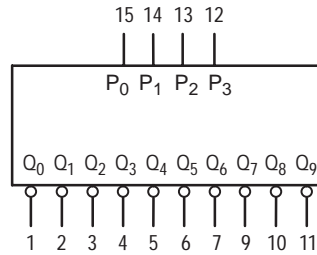
### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
Open Collector	15 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

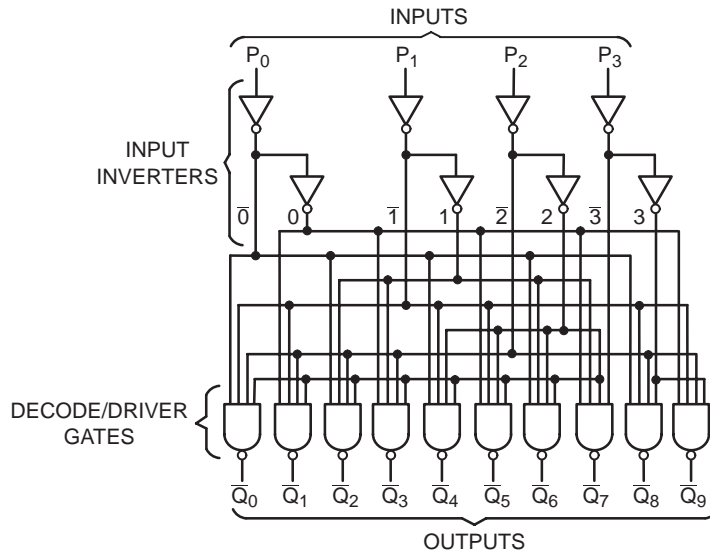
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
 GND = PIN 8

# SN74LS145

## LOGIC DIAGRAM



## TRUTH TABLE

INPUTS				OUTPUTS									
P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>	$\bar{Q}_0$	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	$\bar{Q}_6$	$\bar{Q}_7$	$\bar{Q}_8$	$\bar{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level



# SN74LS145

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$I_{OH}$	Output HIGH Current			250	$\mu\text{A}$	$V_{CC} = \text{MIN}$ , $V_{OH} = \text{MAX}$
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$
			2.3	3.0	V	$I_{OL} = 80 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{CC}$	Power Supply Current			13	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = \text{GND}$

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PHL}$ $t_{PLH}$	Propagation Delay $P_n$ Input to $Q_n$ Output			50 50	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$

## AC WAVEFORMS

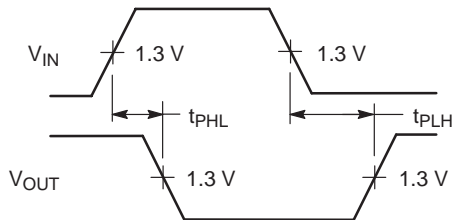


Figure 1.

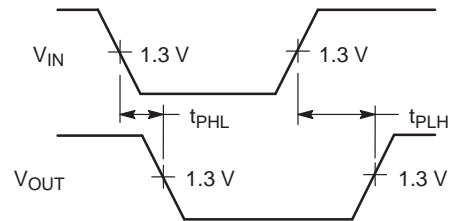


Figure 2.

# SN74LS147 SN74LS148

## 10-Line-to-4-Line and 8-Line-to-3-Line Priority Encoders

The SN74LS147 and the SN74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

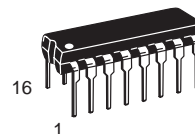
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

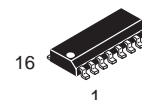


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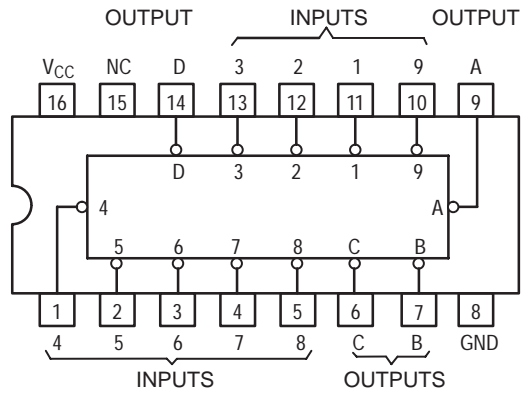
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

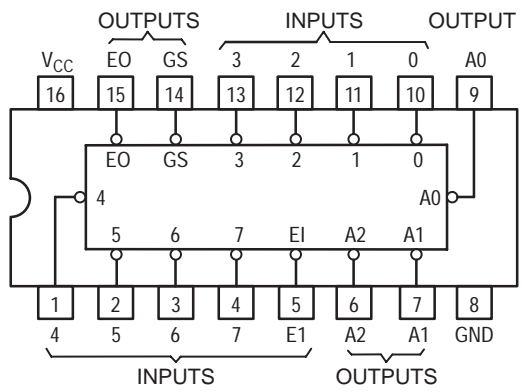
Device	Package	Shipping
SN74LS147N	16 Pin DIP	2000 Units/Box
SN74LS147D	16 Pin	2500/Tape & Reel
SN74LS148N	16 Pin DIP	2000 Units/Box
SN74LS148D	16 Pin	2500/Tape & Reel

# SN74LS147 SN74LS148

**SN74LS147**  
(TOP VIEW)



**SN74LS148**  
(TOP VIEW)



# SN74LS147 SN74LS148

**SN74LS147  
FUNCTION TABLE**

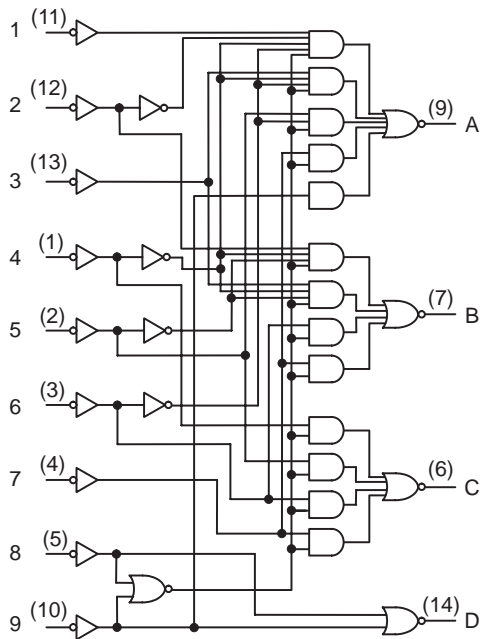
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	L	H
X	X	X	L	H	H	H	H	H	H	L	H	L
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

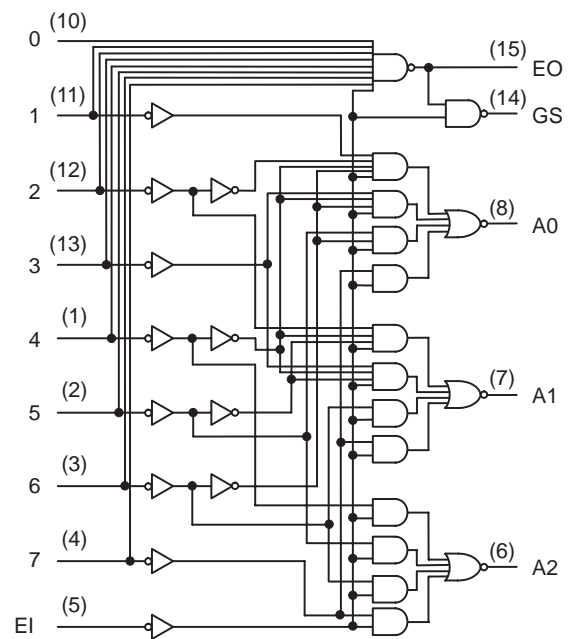
**SN74LS148  
FUNCTION TABLE**

INPUTS								OUTPUTS					
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	H	H	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

## FUNCTIONAL BLOCK DIAGRAMS



**SN74LS147**



**SN74LS148**

## SN74LS147 SN74LS148

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current All Others Inputs 1-7 (LS148)			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	All Others Inputs 1-7 (LS148)			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current All Others Inputs 1-7 (LS148)			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CCH</sub>	Power Supply Current Output HIGH			17	mA	V <sub>CC</sub> = MAX, All Inputs = 4.5 V
I <sub>CCL</sub>	Output LOW			20	mA	V <sub>CC</sub> = MAX, Inputs 7 & E1 = GND All Other Inputs = 4.5 V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## SN74LS147 SN74LS148

AC CHARACTERISTICS ( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

### SN74LS147

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	Test Conditions
				Min	Typ	Max		
$t_{PLH}$	Any	Any	In-phase output		12	18	ns	$C_L = 15\text{ pF}$ , $R_L = 2.0\text{ k}\Omega$
$t_{PHL}$					12	18		
$t_{PLH}$	Any	Any	Out-of-phase output		21	33	ns	
$t_{PHL}$					15	23		

### SN74LS148

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	Test Conditions	
				Min	Typ	Max			
$t_{PLH}$	1 thru 7	A0, A1, or A2	In-phase output		14	18	ns	$C_L = 15\text{ pF}$ , $R_L = 2.0\text{ k}\Omega$	
$t_{PHL}$					15	25			
$t_{PLH}$	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36	ns		
$t_{PHL}$					16	29			
$t_{PLH}$	0 thru 7	EO	Out-of-phase output		7.0	18	ns		
$t_{PHL}$					25	40			
$t_{PLH}$	0 thru 7	GS	In-phase output		35	55	ns		
$t_{PHL}$					9.0	21			
$t_{PLH}$	EI	A0, A1, or A2	In-phase output		16	25	ns		
$t_{PHL}$					12	25			
$t_{PLH}$	EI	GS	In-phase output		12	17	ns		
$t_{PHL}$					14	36			
$t_{PLH}$	EI	EO	In-phase output		12	21	ns		
$t_{PHL}$					28	40			
					30	45			(LS148)

# SN74LS151

## 8-Input Multiplexer

The TTL/MSI SN74LS151 is a high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

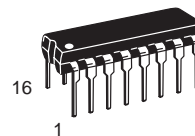
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

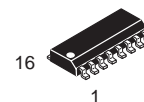


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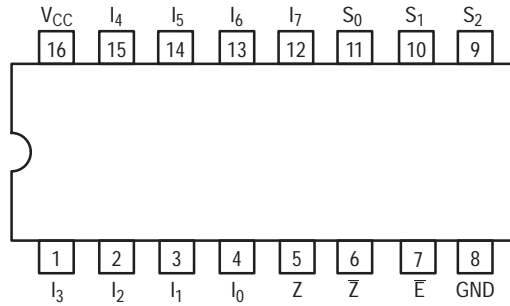
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS151N	16 Pin DIP	2000 Units/Box
SN74LS151D	16 Pin	2500/Tape & Reel

# SN74LS151

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

$S_0 - S_2$	Select Inputs
$\bar{E}$	Enable (Active LOW) Input
$I_0 - I_7$	Multiplexer Inputs
Z	Multiplexer Output
$\bar{Z}$	Complementary Multiplexer Output

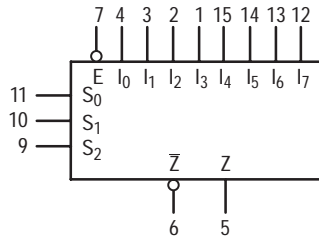
### LOADING (Note a)

	HIGH	LOW
$S_0 - S_2$	0.5 U.L.	0.25 U.L.
$\bar{E}$	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	0.5 U.L.	0.25 U.L.
Z	10 U.L.	5 U.L.
$\bar{Z}$	10 U.L.	5 U.L.

### NOTES:

- 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 5 U.L. for Commercial (74) Temperature Ranges.

## LOGIC SYMBOL

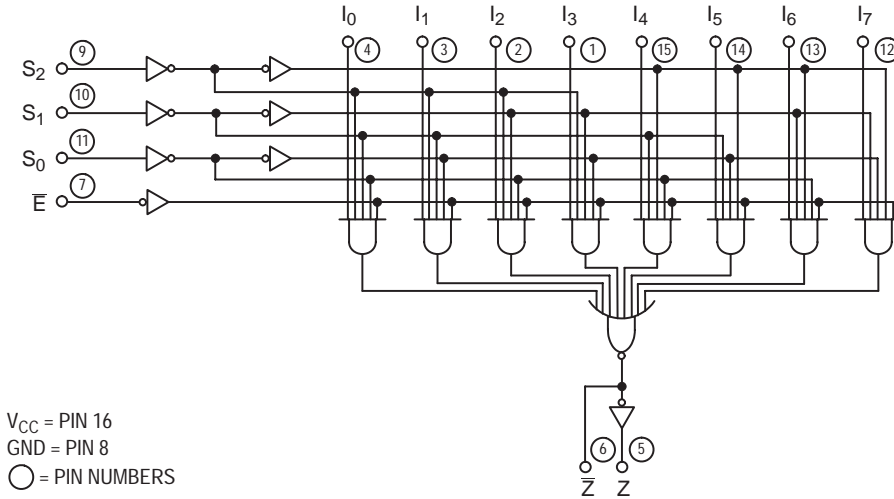


$V_{CC}$  = PIN 16  
GND = PIN 8



# SN74LS151

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Enable input ( $\bar{E}$ ) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

### TRUTH TABLE

$\bar{E}$	$S_2$	$S_1$	$S_0$	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

# SN74LS151

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Select to Output Z		27 18	43 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay Select to Output $\bar{Z}$		14 20	23 32	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output Z		26 20	42 32	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output $\bar{Z}$		15 18	24 30	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output Z		20 16	32 26	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output $\bar{Z}$		13 12	21 20	ns	

## AC WAVEFORMS

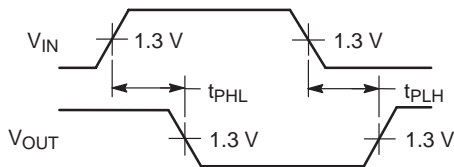


Figure 1.

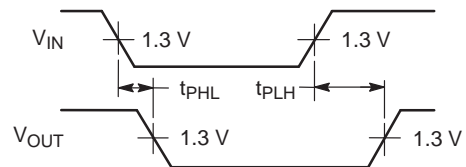


Figure 2.

# SN74LS153

## Dual 4-Input Multiplexer

The LSTTL/MSI SN74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Multifunction Capability
- Non-Inverting Outputs
- Separate Enable for Each Multiplexer
- Input Clamp Diodes Limit High Speed Termination Effects

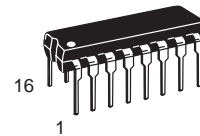
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

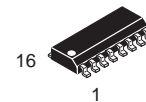


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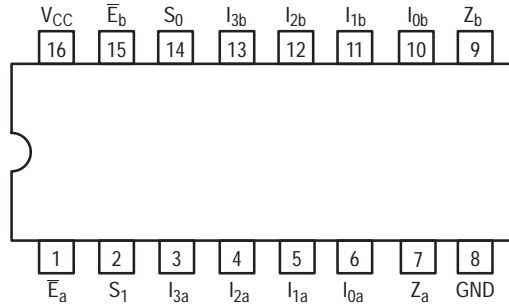
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS153N	16 Pin DIP	2000 Units/Box
SN74LS153D	16 Pin	2500/Tape & Reel

# SN74LS153

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$S_0$	Common Select Input
$\bar{E}$	Enable (Active LOW) Input
$I_0, I_1$	Multiplexer Inputs
$Z$	Multiplexer Output

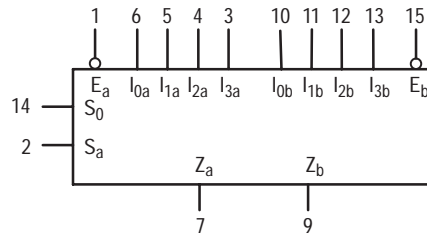
### LOADING (Note a)

	HIGH	LOW
$S_0$	0.5 U.L.	0.25 U.L.
$\bar{E}$	0.5 U.L.	0.25 U.L.
$I_0, I_1$	0.5 U.L.	0.25 U.L.
$Z$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

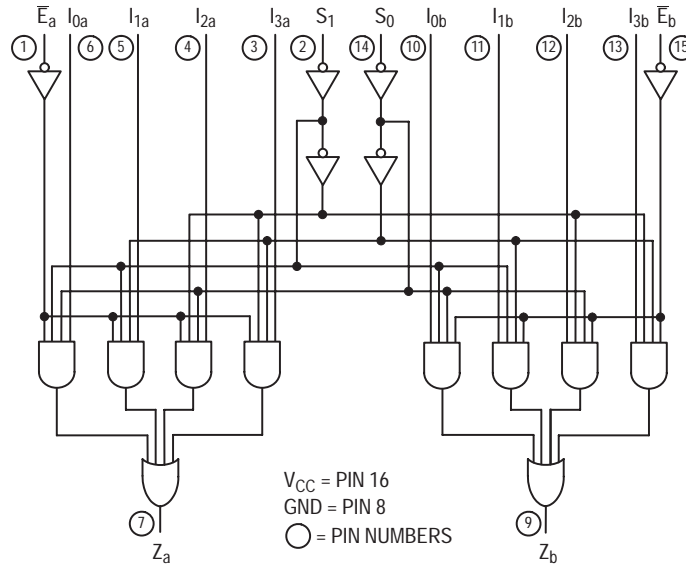
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS153

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS153 is a Dual 4-input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $\bar{E}_a, \bar{E}_b$ ) which can be used to strobe the outputs independently. When the Enables ( $\bar{E}_a, \bar{E}_b$ ) are HIGH, the corresponding outputs ( $Z_a, Z_b$ ) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

### TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
$S_0$	$S_1$	$\bar{E}$	$I_0$	$I_1$	$I_2$	$I_3$	$Z$
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

# SN74LS153

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output		10 17	15 26	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay Select to Output		19 25	29 38	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output		16 21	24 32	ns	

## AC WAVEFORMS

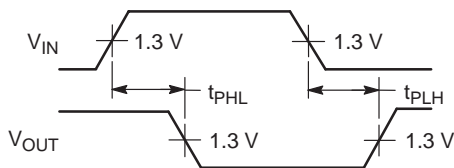


Figure 1.

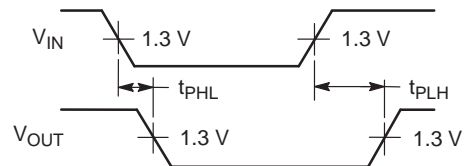


Figure 2.

# SN74LS156

## Dual 1-of-4 Decoder/ Demultiplexer

The SN74LS156 is a high speed Dual 1-of-4 Decoder/Demultiplexer. This device has two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS156 is fabricated with the Schottky barrier diode process for high speed and are completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
V <sub>OH</sub>	Output Voltage – High			5.5	V
I <sub>OL</sub>	Output Current – Low			8.0	mA

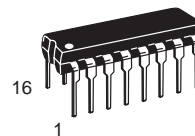


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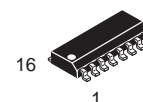
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### LS156–OPEN–COLLECTOR LOW POWER SCHOTTKY



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CASE 648



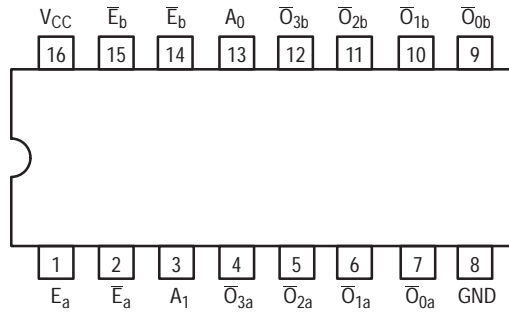
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS156N	16 Pin DIP	2000 Units/Box
SN74LS156D	16 Pin	2500/Tape & Reel

# SN74LS156

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$A_0, A_1$	Address Inputs
$\bar{E}_a, \bar{E}_b$	Enable (Active LOW) Inputs
$E_a$	Enable (Active HIGH) Input
$\bar{O}_0 - \bar{O}_3$	Active LOW Outputs

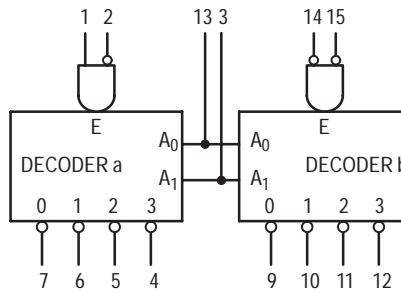
### LOADING (Note a)

	HIGH	LOW
$A_0, A_1$	0.5 U.L.	0.25 U.L.
$\bar{E}_a, \bar{E}_b$	0.5 U.L.	0.25 U.L.
$E_a$	0.5 U.L.	0.25 U.L.
$\bar{O}_0 - \bar{O}_3$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL

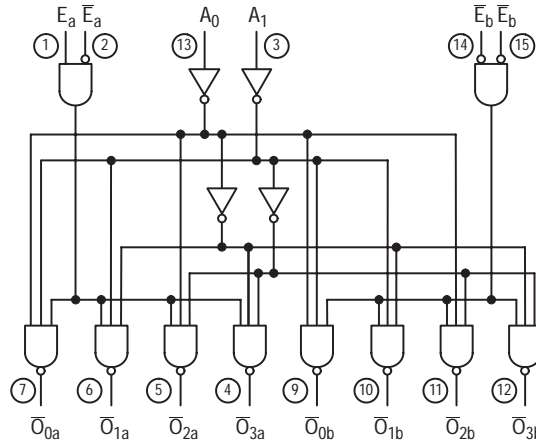


$V_{CC}$  = PIN 16  
GND = PIN 8



# SN74LS156

## LOGIC DIAGRAM



$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

### FUNCTIONAL DESCRIPTION

The LS156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs ( $A_0$ ,  $A_1$ ) and provides four mutually exclusive active LOW outputs ( $\bar{O}_0$ – $\bar{O}_3$ ). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder “a” requires one active HIGH input and one active LOW input ( $E_a \cdot \bar{E}_a$ ). In demultiplexing applications, Decoder “a” can accept either true or complemented data by using the  $\bar{E}_a$  or  $E_a$  inputs respectively. The enable gate for Decoder “b” requires two active LOW inputs ( $\bar{E}_b \cdot \bar{E}_b$ ). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying  $E_a$  to  $\bar{E}_b$  and relabeling the common connection as ( $A_2$ ). The other  $\bar{E}_b$  and  $\bar{E}_a$  are connected together to form the common enable.

The LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in

Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + \bar{A}_0 + \bar{A}_1)$$

where  $E = E_a + \bar{E}_a$ ;  $E = E_b + \bar{E}_b$

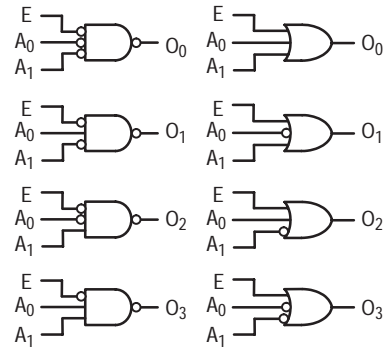


Figure a

### TRUTH TABLE

ADDRESS		ENABLE “a”		OUTPUT “a”				ENABLE “b”		OUTPUT “b”			
$A_0$	$A_1$	$E_a$	$\bar{E}_a$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{E}_b$	$E_b$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

# SN74LS156

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$I_{OH}$	Output HIGH Current			100	$\mu\text{A}$	$V_{CC} = \text{MIN}$ , $V_{OH} = \text{MAX}$
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{CC}$	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address, $\bar{E}_a$ or $\bar{E}_b$ to Output		25 34	40 51	ns	Figure 1
$t_{PLH}$ $t_{PHL}$	Propagation Delay Address to Output		31 34	46 51	ns	Figure 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_a$ to Output		32 32	48 48	ns	Figure 1

$V_{CC} = 5.0 \text{ V}$   
 $C_L = 15 \text{ pF}$   
 $R_L = 2.0 \text{ k}\Omega$

## AC WAVEFORMS

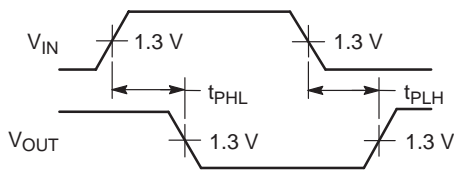


Figure 1.

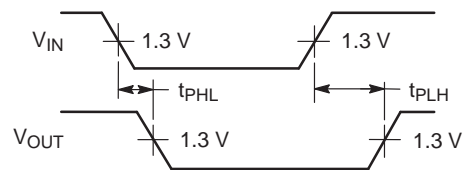


Figure 2.

# SN74LS157

## Quad 2-Input Multiplexer

The LSTTL/MSI SN74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

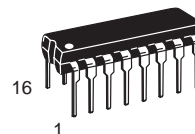
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

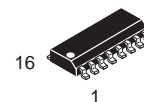


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



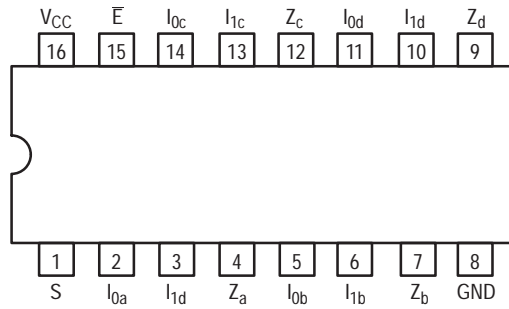
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS157N	16 Pin DIP	2000 Units/Box
SN74LS157D	16 Pin	2500/Tape & Reel

# SN74LS157

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

S	Common Select Input
$\bar{E}$	Enable (Active LOW) Input
$I_{0a} - I_{0d}$	Data Inputs from Source 0
$I_{1a} - I_{1d}$	Data Inputs from Source 1
$Z_a - Z_d$	Multiplexer Outputs

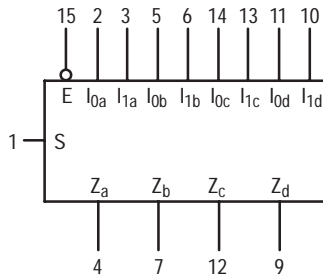
### LOADING (Note a)

	HIGH	LOW
S	1.0 U.L.	0.5 U.L.
$\bar{E}$	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

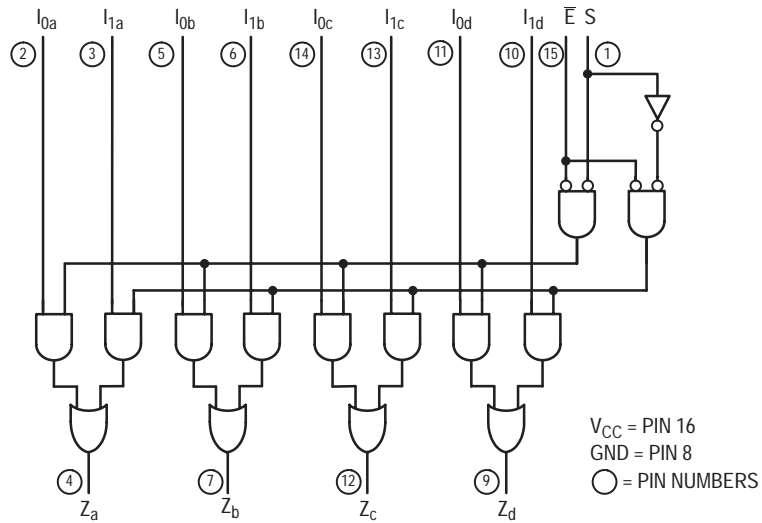
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS157

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \quad Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \quad Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

### TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

# SN74LS157

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current I <sub>0</sub> , I <sub>1</sub> E, S			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	I <sub>0</sub> , I <sub>1</sub> E, S			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current I <sub>0</sub> , I <sub>1</sub> E, S			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			16	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output		9.0 9.0	14 14	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Enable to Output		13 14	20 21	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Select to Output		15 18	23 27	ns	

## AC WAVEFORMS

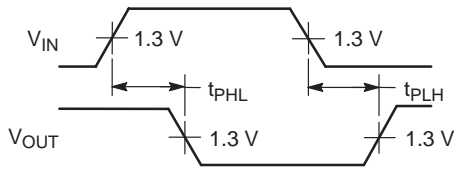


Figure 1.

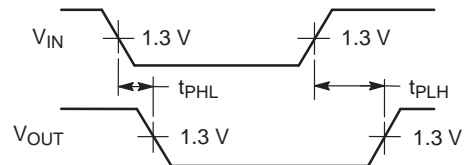


Figure 2.

# SN74LS161A SN74LS163A

## BCD Decade Counters/ 4-Bit Binary Counters

The LS161A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS161A and LS163A count modulo 16 (binary).

The LS161A has an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS163A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	Binary (Modulo 16)
Asynchronous Reset	LS161A
Synchronous Reset	LS163A

- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

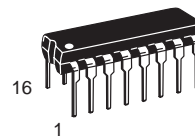
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

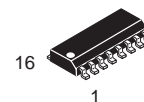


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### LOW POWER SCHOTTKY



**PLASTIC  
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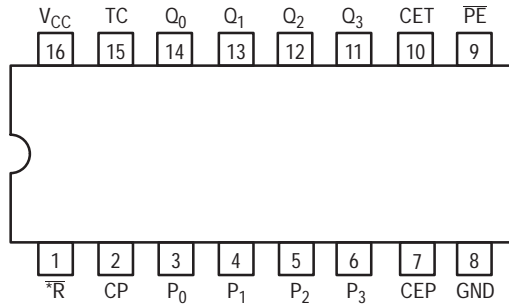
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS161AN	16 Pin DIP	2000 Units/Box
SN74LS161AD	16 Pin	2500/Tape & Reel
SN74LS163AN	16 Pin DIP	2000 Units/Box
SN74LS163AD	16 Pin	2500/Tape & Reel

# SN74LS161A SN74LS163A

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

\*MR for LS161A  
\*SR for LS163A

### PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
$P_0 - P_3$	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{SR}$	Synchronous Reset (Active LOW) Input
$Q_0 - Q_3$	Parallel Outputs
TC	Terminal Count Output

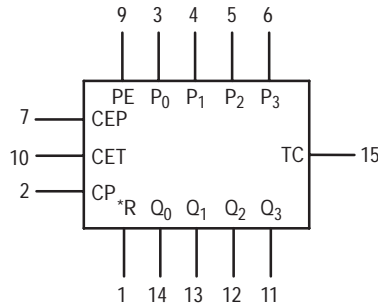
### LOADING (Note a)

	HIGH	LOW
$\overline{PE}$	1.0 U.L.	0.5 U.L.
$P_0 - P_3$	0.5 U.L.	0.25 U.L.
CEP	0.5 U.L.	0.25 U.L.
CET	1.0 U.L.	0.5 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$\overline{SR}$	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
TC	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



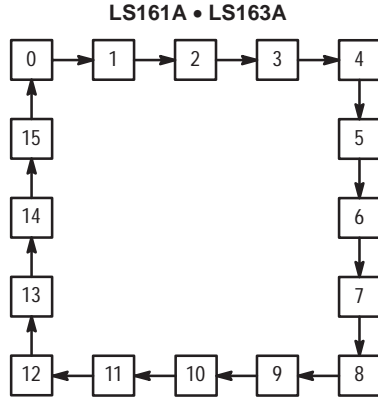
$V_{CC}$  = PIN 16  
GND = PIN 8

\*MR for LS161A  
\*SR for LS163A



# SN74LS161A SN74LS163A

## STATE DIAGRAM



### LOGIC EQUATIONS

Count Enable =  $CEP \cdot CET \cdot PE$

TC for LS161A & LS163A =  $CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

Preset =  $\overline{PE} \cdot CP +$  (rising clock edge)

Reset =  $\overline{MR}$  (LS161A)

Reset =  $\overline{SR} \cdot CP +$  (rising clock edge)  
(LS163A)

## FUNCTIONAL DESCRIPTION

The LS161A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and  $\overline{PE}$  inputs are HIGH. When the  $\overline{PE}$  is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the  $\overline{PE}$  held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs ( $CET \cdot CEP$ ) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ( $\overline{MR}$ ) of the LS161A is asynchronous. When the  $\overline{MR}$  is LOW, it overrides all other input conditions and sets the outputs LOW. The  $\overline{MR}$  pin should never be left open. If not used, the  $\overline{MR}$  pin should be tied through a resistor to  $V_{CC}$ , or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ( $\overline{SR}$ ) input of the LS163A acts as an edge-triggered control input, overriding CET, CEP and  $\overline{PE}$ , and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge ( $\uparrow$ )
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ( $P_n$ $Q_n$ )
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

\*For the LS163A only.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

# SN74LS161A SN74LS163A

## LS161A

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current MR, Data, CEP, Clock PE, CET			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current MR, Data, CEP, Clock PE, CET			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## LS163A

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current Data, CEP, Clock PE, CET, SR			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Data, CEP, Clock PE, CET, SR			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Data, CEP, Clock, PE, SR CET			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS161A SN74LS163A

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	32		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to TC		20 18	35 35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Q		13 18	24 27	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t <sub>PHL</sub>	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>WCP</sub>	Clock Pulse Width Low	25			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	$\overline{MR}$ or $\overline{SR}$ Pulse Width	20			ns	
t <sub>s</sub>	Setup Time, other*	20			ns	
t <sub>s</sub>	Setup Time PE or SR	25			ns	
t <sub>h</sub>	Hold Time, data	3			ns	
t <sub>h</sub>	Hold Time, other	0			ns	
t <sub>rec</sub>	Recovery Time $\overline{MR}$ to CP	15			ns	

\*CEP, CET, or DATA

## DEFINITION OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

## AC WAVEFORMS

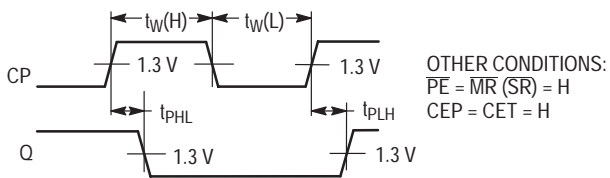


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

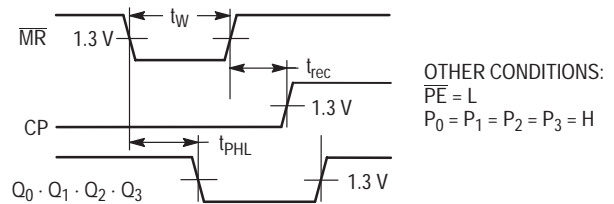


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

# SN74LS161A SN74LS163A

## AC WAVEFORMS (continued)

### COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ( $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ ) state for the LS161 and LS163.

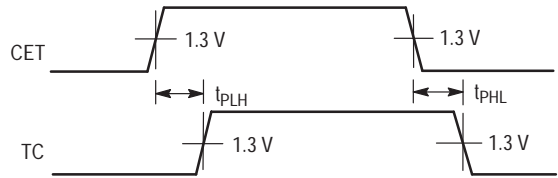


Figure 3.

OTHER CONDITIONS:  $CP = \overline{PE} = CEP = \overline{MR} = H$

### CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state ( $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ ) for the LS161 and LS163.

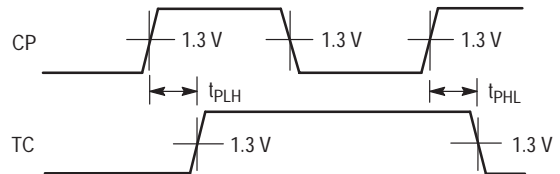


Figure 4.

OTHER CONDITIONS:  $\overline{PE} = CEP = CET = \overline{MR} = H$

### SETUP TIME ( $t_s$ ) AND HOLD TIME ( $t_h$ ) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

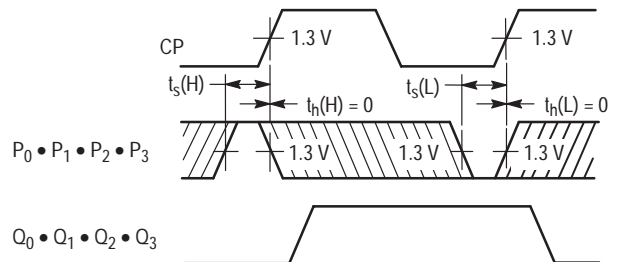


Figure 5.

OTHER CONDITIONS:  $\overline{PE} = L, \overline{MR} = H$

### SETUP TIME ( $t_s$ ) AND HOLD TIME ( $t_h$ ) FOR COUNT ENABLE ( $CEP$ ) AND ( $CET$ ) AND PARALLEL ENABLE ( $\overline{PE}$ ) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

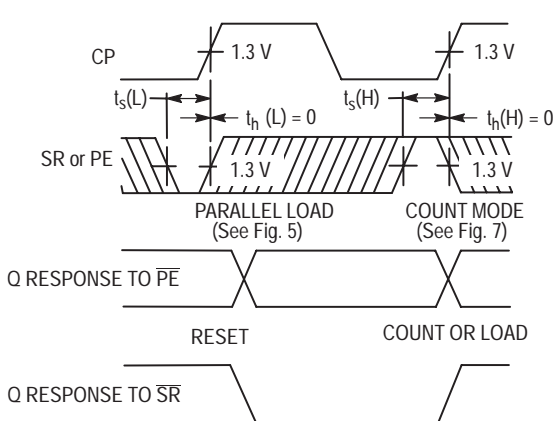


Figure 6.

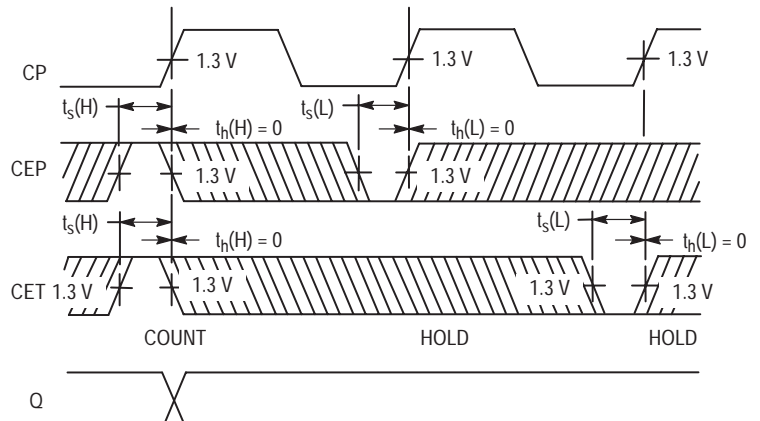


Figure 7.

OTHER CONDITIONS:  $\overline{PE} = H, \overline{MR} = H$

# SN74LS164

## Serial-In Parallel-Out Shift Register

The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

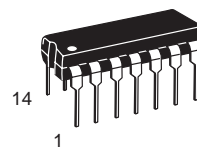
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

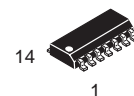


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 646**



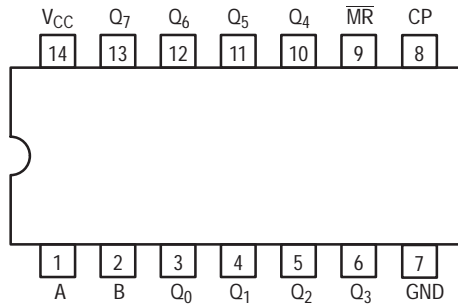
**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS164N	14 Pin DIP	2000 Units/Box
SN74LS164D	14 Pin	2500/Tape & Reel

# SN74LS164

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

A, B	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$Q_0 - Q_7$	Outputs

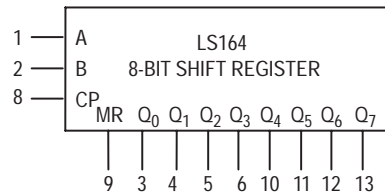
### LOADING (Note a)

	HIGH	LOW
A, B	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

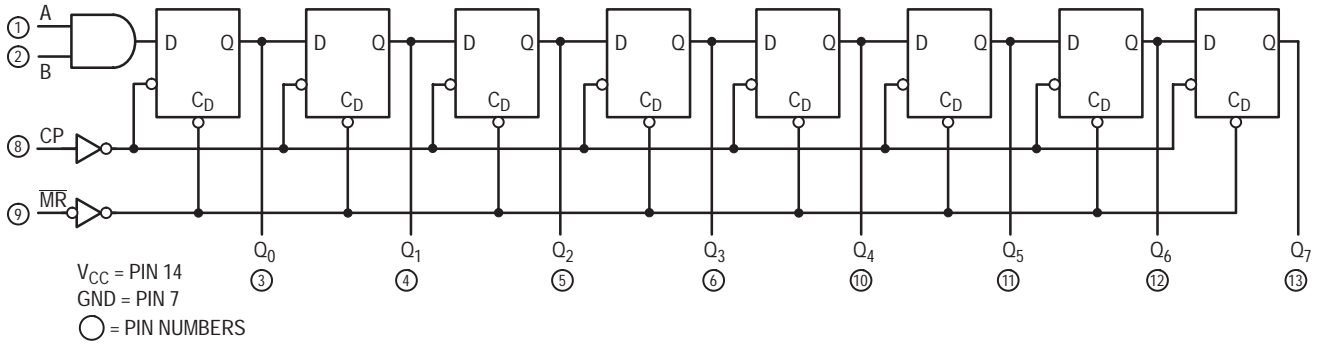
### LOGIC SYMBOL



$V_{CC}$  = PIN 14  
GND = PIN 7

# SN74LS164

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into  $Q_0$  the logical AND of the two data inputs ( $A \bullet B$ ) that existed before the rising clock edge. A LOW level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

### MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	$Q_0$	$Q_1-Q_7$
Reset (Clear)	L	X	X	L	L - L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels

H (h) = HIGH Voltage Levels

X = Don't Care

$q_n$  = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

# SN74LS164

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			27	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	36		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Propagation Delay MR to Output Q		24	36	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output Q		17 21	27 32	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

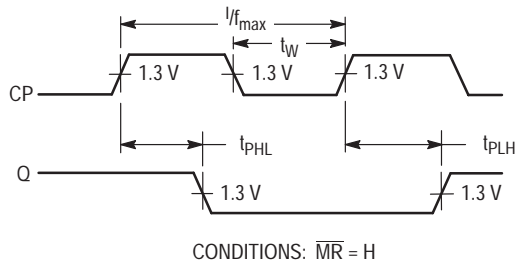
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP, MR Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time	15			ns	
t <sub>h</sub>	Data Hold Time	5.0			ns	
t <sub>rec</sub>	MR to Clock Recovery Time	20			ns	



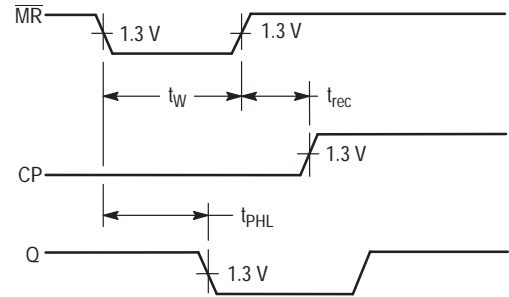
# SN74LS164

## AC WAVEFORMS

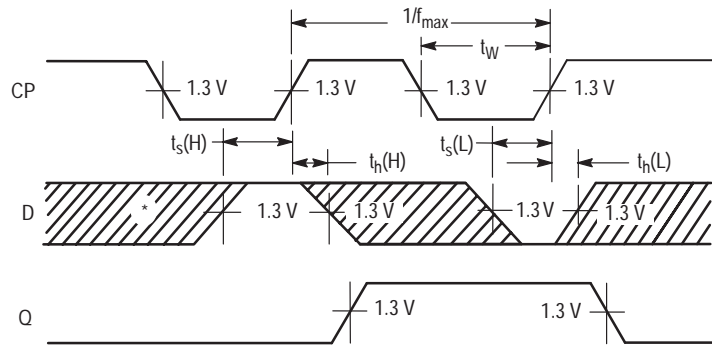
\*The shaded areas indicate when the input is permitted to change for predictable output performance.



**Figure 1. Clock to Output Delays and Clock Pulse Width**



**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



**Figure 3. Data Setup and Hold Times**

# SN74LS165

## 8-Bit Parallel-to-Serial Shift Register

The SN74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ( $\overline{PL}$ ) input is LOW. With  $\overline{PL}$  HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

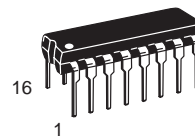
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

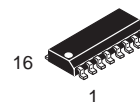


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### LOW POWER SCHOTTKY



PLASTIC  
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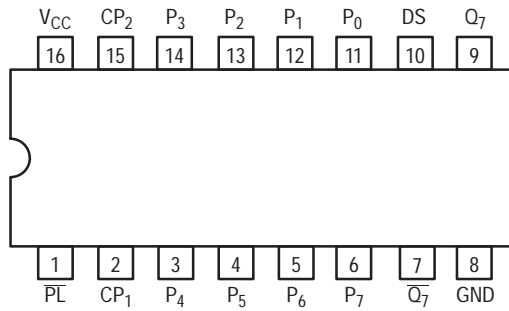
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS165N	16 Pin DIP	2000 Units/Box
SN74LS165D	16 Pin	2500/Tape & Reel

# SN74LS165

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CP <sub>1</sub> , CP <sub>2</sub>	Clock (LOW-to-HIGH Going Edge) Inputs
DS	Serial Data Input
PL	Asynchronous Parallel Load (Active LOW) Input
P <sub>0</sub> – P <sub>7</sub>	Parallel Data Inputs
Q <sub>7</sub>	Serial Output from Last State
Q <sub>7</sub>	Complementary Output

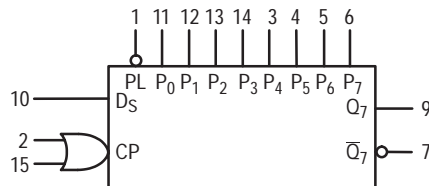
### LOADING (Note a)

	HIGH	LOW
CP <sub>1</sub> , CP <sub>2</sub>	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
PL	1.5 U.L.	0.75 U.L.
P <sub>0</sub> – P <sub>7</sub>	0.5 U.L.	0.25 U.L.
Q <sub>7</sub>	10 U.L.	5 U.L.
Q <sub>7</sub>	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

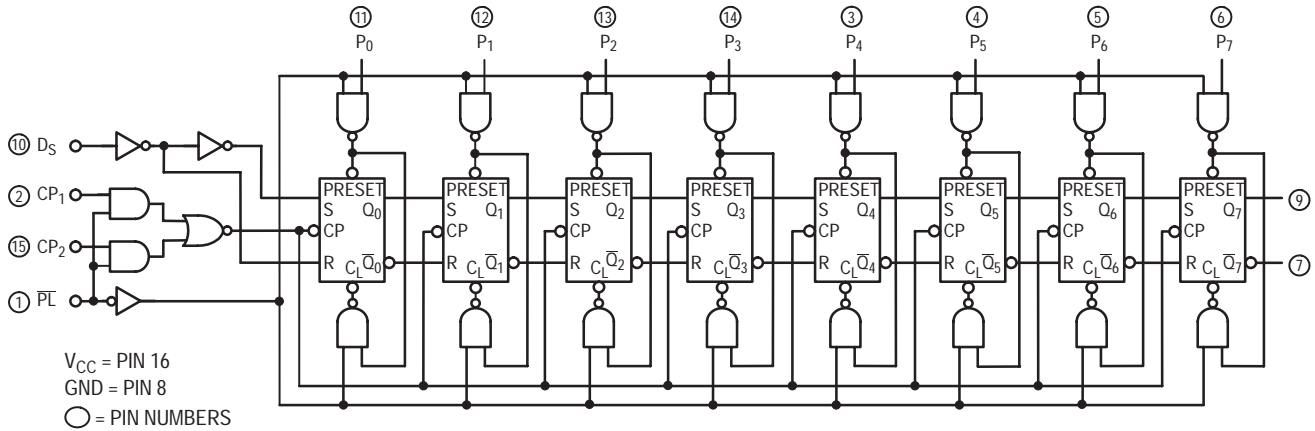
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN74LS165

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The SN74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the  $\overline{PL}$  signal is LOW. The parallel data can change while  $\overline{PL}$  is LOW, provided that the recommended setup and hold times are observed.

For clock operation,  $\overline{PL}$  must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit

by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

### TRUTH TABLE

$\overline{PL}$	CP		CONTENTS								RESPONSE
	1	2	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	
L	X	X	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>	Parallel Entry
H	L		D <sub>S</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H	H		Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change
H		L	D <sub>S</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H		H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

# SN74LS165

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current Other Inputs P <sub>L</sub> Input			20 60	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Other Inputs P <sub>L</sub> Input			0.1 0.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Other Inputs P <sub>L</sub> Input			-0.4 -1.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			36	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	25	35		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>L</sub> to Output		22 22	35 35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output		27 28	40 40	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>		14 21	25 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>		21 16	30 25	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP Clock Pulse Width	25			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	P <sub>L</sub> Pulse Width	15			ns	
t <sub>S</sub>	Parallel Data Setup Time	10			ns	
t <sub>S</sub>	Serial Data Setup Time	20			ns	
t <sub>S</sub>	CP <sub>1</sub> to CP <sub>2</sub> Setup Time <sup>1</sup>	30			ns	
t <sub>H</sub>	Hold Time	0			ns	
t <sub>rec</sub>	Recovery Time, P <sub>L</sub> to CP	45			ns	

<sup>1</sup>The role of CP<sub>1</sub> and CP<sub>2</sub> in an application may be interchanged.

**DEFINITION OF TERMS:**

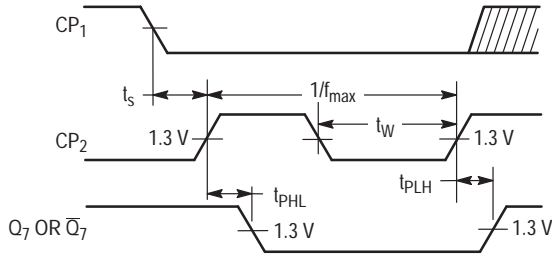
**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure

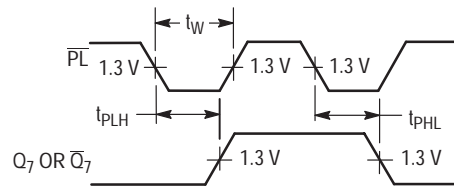
continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the  $\overline{PL}$  pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

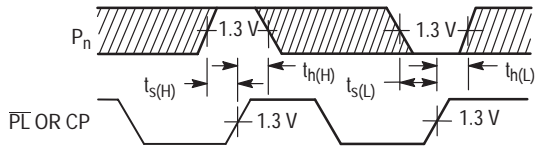
**AC WAVEFORMS**



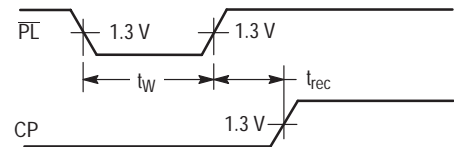
**Figure 1.**



**Figure 2.**



**Figure 3.**



**Figure 4.**

# SN74LS166

## 8-Bit Shift Registers

The SN74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

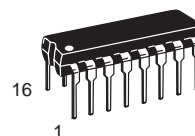
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

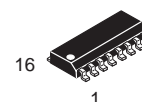


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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648

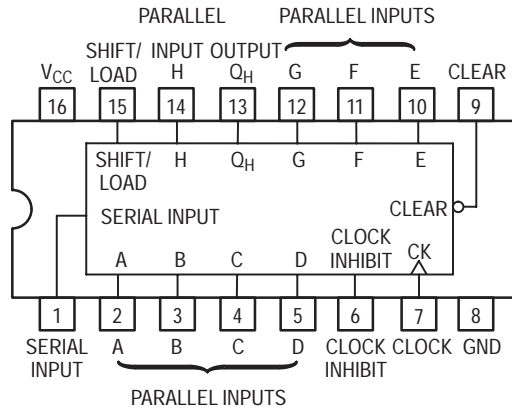


SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS166N	16 Pin DIP	2000 Units/Box
SN74LS166D	16 Pin	2500/Tape & Reel

# SN74LS166



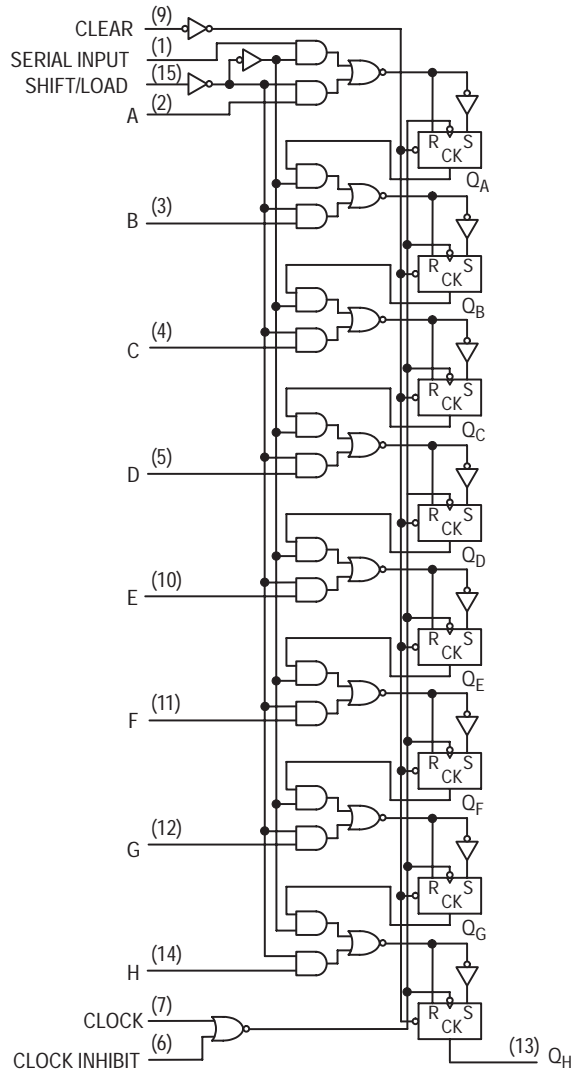
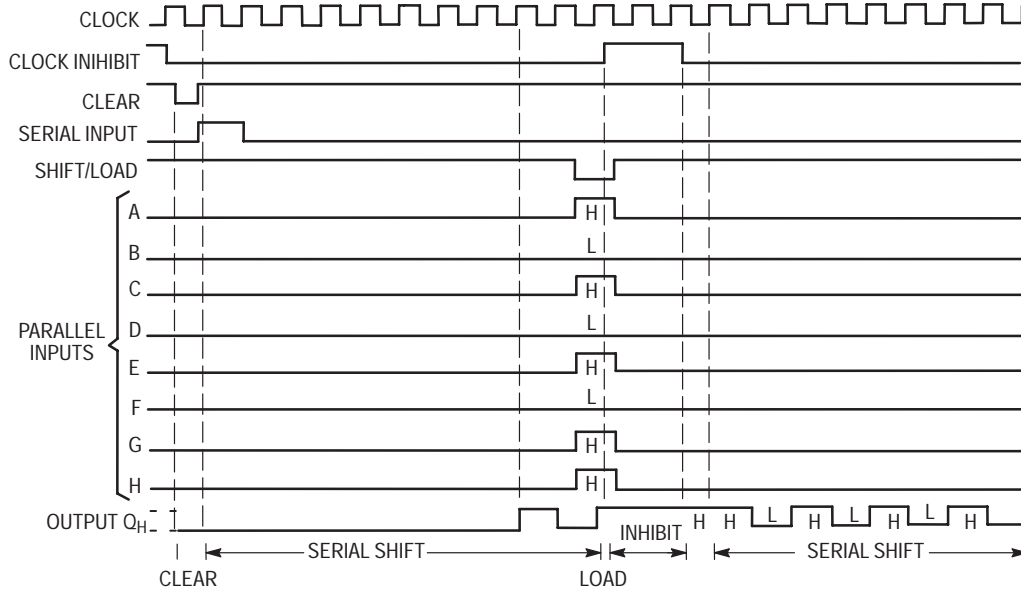
**FUNCTION TABLE**

INPUTS						INTERNAL OUTPUTS		OUTPUT Q <sub>H</sub>
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL	Q <sub>A</sub>	Q <sub>B</sub>	
					A . . . H			
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>



# SN74LS166

## Typical Clear, Shift, Load, Inhibit, and Shift Sequences



# SN74LS166

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			38	mA	$V_{CC} = \text{MAX}$

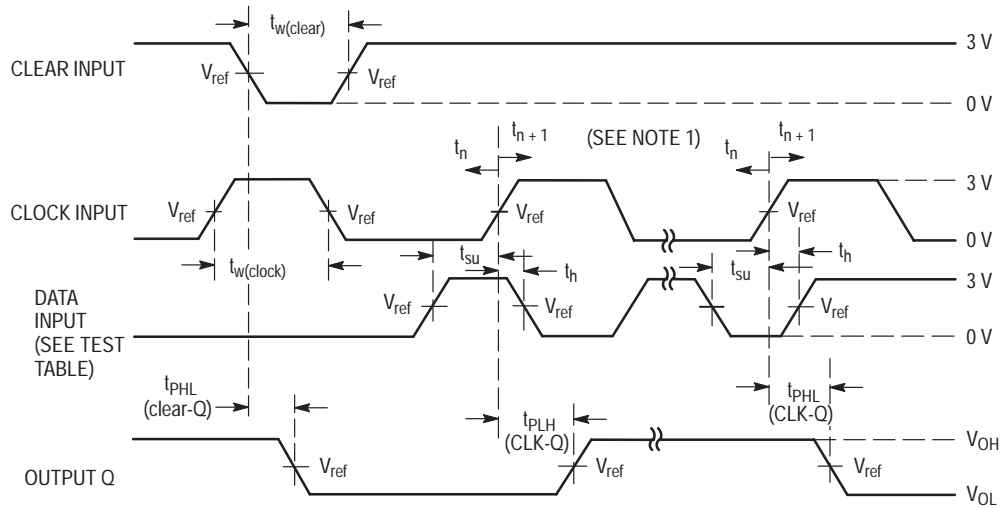
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS166

## TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0 V	$Q_H$ at $t_{n+1}$
Serial Input	4.5 V	$Q_H$ at $t_{n+8}$

## AC WAVEFORMS



NOTE 1.  $t_n$  = bit time before clocking transition  
 $t_{n+1}$  = bit time after one clocking transition  
 $t_{n+8}$  = bit time after eight clocking transition  
 LS166  $V_{ref} = 1.3$  V.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Clock Frequency	25	35		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
$t_{PHL}$	Clear to Output		19	30	ns	
$t_{PLH}$ $t_{PHL}$	Clock to Output		23 24	35 35	ns	

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock Clear Pulse Width	30			ns	$V_{CC} = 5.0$ V
$t_s$	Mode Control Setup Time	30			ns	
$t_s$	Data Setup Time	20			ns	
$t_h$	Hold Time, Any Input	15			ns	

# SN74LS174

## Hex D Flip-Flop

The LSTTL/MSI SN74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Asynchronous Common Reset
- Input Clamp Diodes Limit High Speed Termination Effects

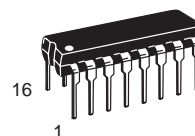
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

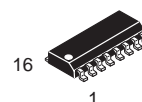


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



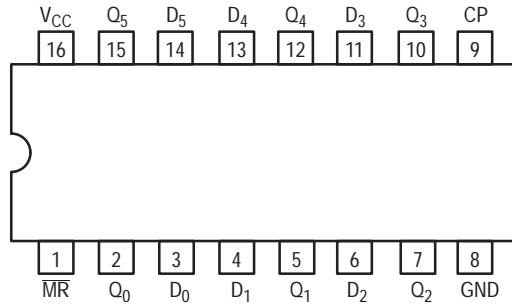
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS174N	16 Pin DIP	2000 Units/Box
SN74LS174D	16 Pin	2500/Tape & Reel

# SN74LS174

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

D <sub>0</sub> – D <sub>5</sub>	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q <sub>0</sub> – Q <sub>5</sub>	Outputs

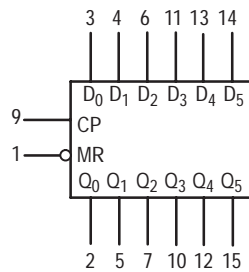
### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 U.L.

### NOTES:

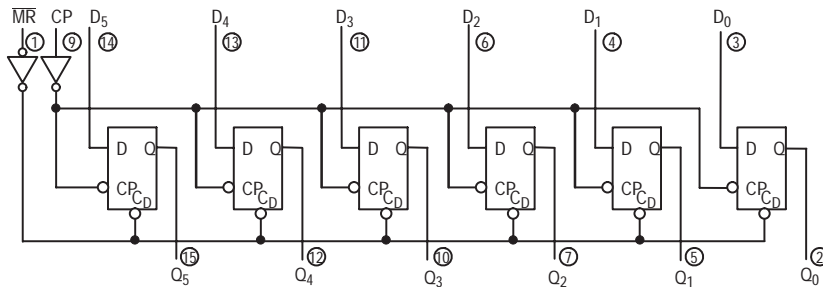
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

### LOGIC DIAGRAM



V<sub>CC</sub> = PIN 16  
GND = PIN 8  
○ = PIN NUMBERS

# SN74LS174

## FUNCTIONAL DESCRIPTION

The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ( $\overline{MR}$ ) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ( $\overline{MR}$ ) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR} = H$ )	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			26	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS174

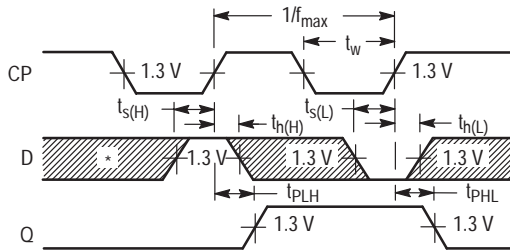
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	30	40		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Propagation Delay, $\overline{MR}$ to Output		23	35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		20 21	30 30	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

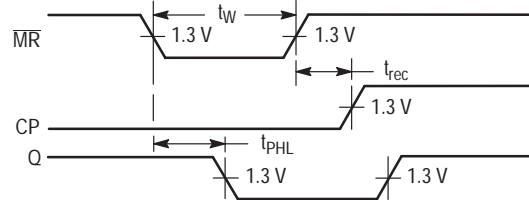
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock or MR Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time	20			ns	
t <sub>h</sub>	Data Hold Time	5.0			ns	
t <sub>rec</sub>	Recovery Time	25			ns	

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

## DEFINITIONS OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

# SN74LS175

## Quad D Flip-Flop

The LSTTL/MSI SN74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

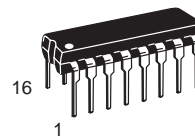
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

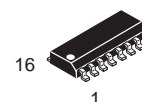


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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648



SOIC  
D SUFFIX  
CASE 751B

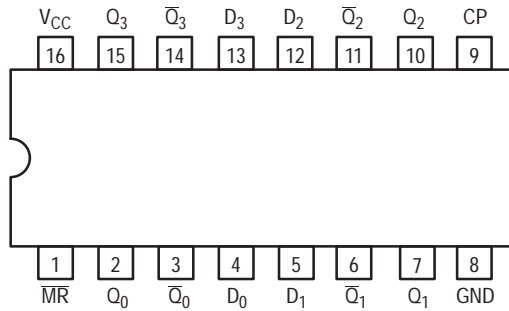
### ORDERING INFORMATION

Device	Package	Shipping
SN74LS175N	16 Pin DIP	2000 Units/Box
SN74LS175D	16 Pin	2500/Tape & Reel



# SN74LS175

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$D_0 - D_3$	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$Q_0 - Q_3$	True Outputs
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs

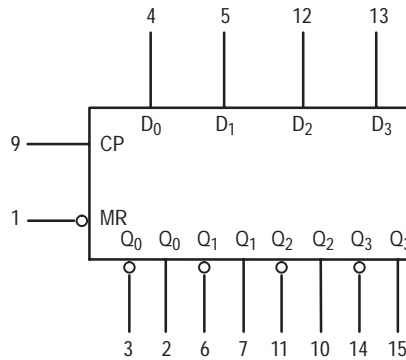
### LOADING (Note a)

	HIGH	LOW
$D_0 - D_3$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
$\overline{Q}_0 - \overline{Q}_3$	10 U.L.	5 U.L.

### NOTES:

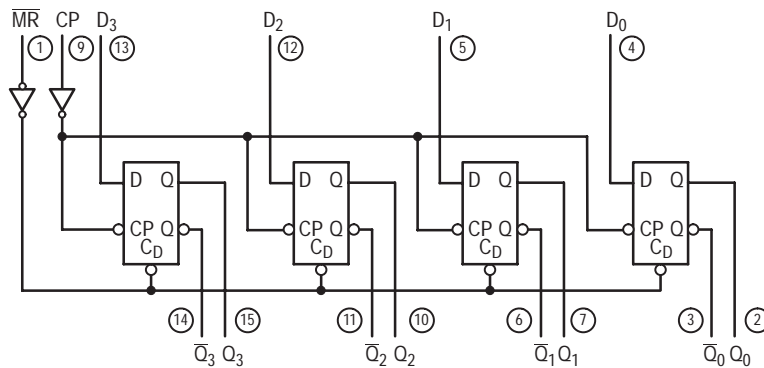
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

### LOGIC DIAGRAM



$V_{CC}$  = PIN 16  
GND = PIN 8

○ = PIN NUMBERS

# SN74LS175

## FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to

follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\bar{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			18	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS175

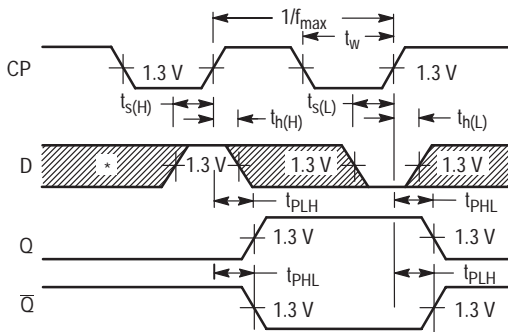
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	30	40		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\overline{MR}$ to Output		20 20	30 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		13 16	25 25	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

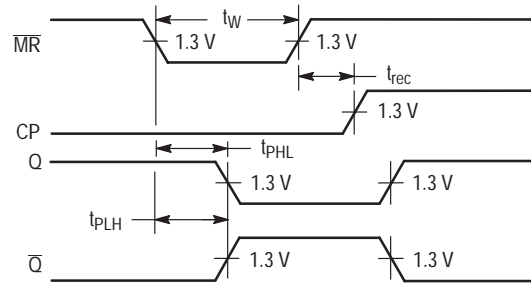
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock or $\overline{MR}$ Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time	20			ns	
t <sub>h</sub>	Data Hold Time	5.0			ns	
t <sub>rec</sub>	Recovery Time	25			ns	

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

## DEFINITIONS OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

# SN74LS193

## Presettable 4-Bit Binary Up/Down Counter

The SN74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and the circuits can operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ( $\overline{PL}$ ) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects

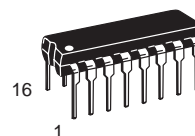
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

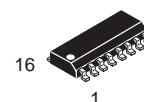


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



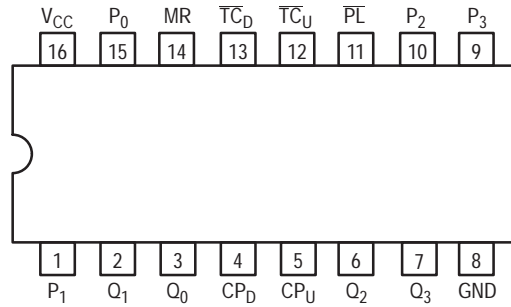
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS193N	16 Pin DIP	2000 Units/Box
SN74LS193D	16 Pin	2500/Tape & Reel

# SN74LS193

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CP <sub>U</sub>	Count Up Clock Pulse Input
CP <sub>D</sub>	Count Down Clock Pulse Input
MR	Asynchronous Master Reset (Clear) Input
PL	Asynchronous Parallel Load (Active LOW) Input
P <sub>n</sub>	Parallel Data Inputs
Q <sub>n</sub>	Flip-Flop Outputs
TC <sub>D</sub>	Terminal Count Down (Borrow) Output
TC <sub>U</sub>	Terminal Count Up (Carry) Output

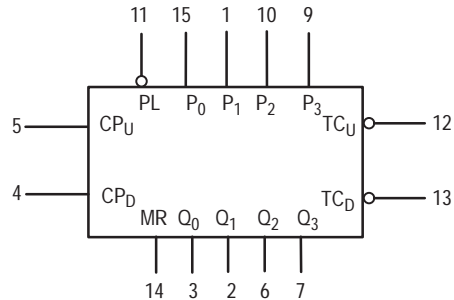
### LOADING (Note a)

	HIGH	LOW
CP <sub>U</sub>	0.5 U.L.	0.25 U.L.
CP <sub>D</sub>	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
PL	0.5 U.L.	0.25 U.L.
P <sub>n</sub>	0.5 U.L.	0.25 U.L.
Q <sub>n</sub>	10 U.L.	5 U.L.
TC <sub>D</sub>	10 U.L.	5 U.L.
TC <sub>U</sub>	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

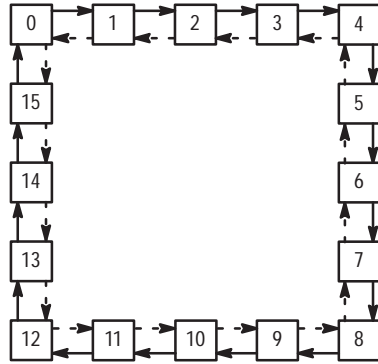
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN74LS193

## STATE DIAGRAM



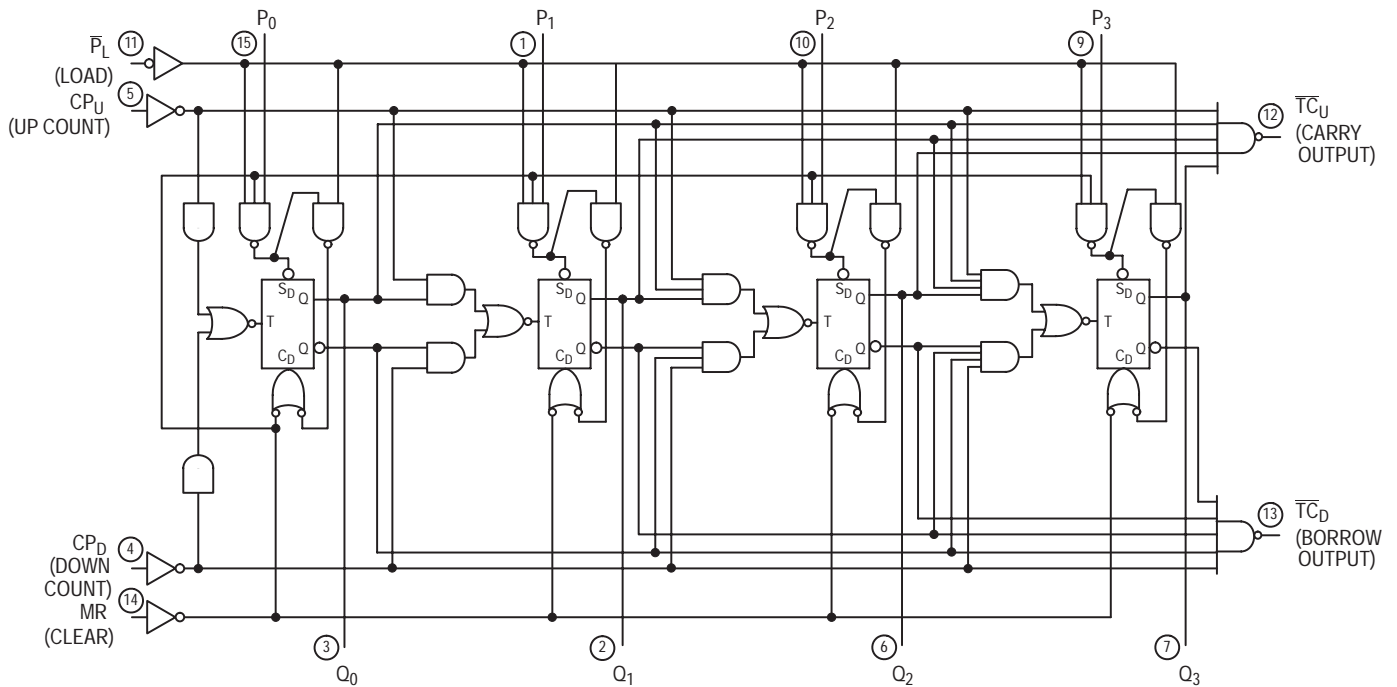
### LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CP_D$$

COUNT UP ———  
 COUNT DOWN - - - -

## LOGIC DIAGRAM



$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

**FUNCTIONAL DESCRIPTION**

The LS193 is a 4-Bit Binary Synchronous UP/DOWN (Reversible) Counter. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ( $\overline{TC}_U$ ) and Terminal Count Down ( $\overline{TC}_D$ ) outputs are normally HIGH. When a circuit has

reached the maximum count state of 15, the next HIGH-to-LOW transition of the Count Up Clock will cause  $\overline{TC}_U$  to go LOW.  $\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the  $\overline{TC}_D$  output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ( $\overline{PL}$ ) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs ( $P_0, P_3$ ) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

**MODE SELECT TABLE**

MR	$\overline{PL}$	$CP_U$	$CP_D$	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	$\uparrow$	H	Count Up
L	H	H	$\downarrow$	Count Down

L = LOW Voltage Level  
 H = HIGH Voltage Level  
 X = Don't Care  
 $\uparrow$  = LOW-to-HIGH Clock Transition

# SN74LS193

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			34	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	32		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>U</sub> Input to TC <sub>U</sub> Output		17 18	26 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	CP <sub>D</sub> Input to TC <sub>D</sub> Output		16 15	24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock to Q		27 30	38 47	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	PL to Q		24 25	40 40	ns	
t <sub>PHL</sub>	MR Input to Any Output		23	35	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Any Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time	20			ns	
t <sub>h</sub>	Data Hold Time	5.0			ns	
t <sub>rec</sub>	Recovery Time	40			ns	

## DEFINITIONS OF TERMS

SETUP TIME (t<sub>s</sub>) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the PL transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t<sub>h</sub>) is defined as the minimum time following the PL transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the PL transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t<sub>rec</sub>) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.



# SN74LS193

## AC WAVEFORMS

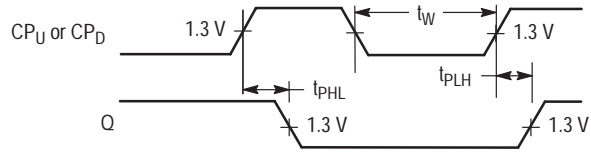


Figure 1.

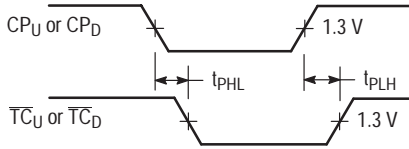
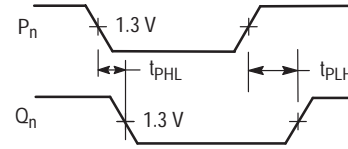


Figure 2.



NOTE: PL = LOW

Figure 3.

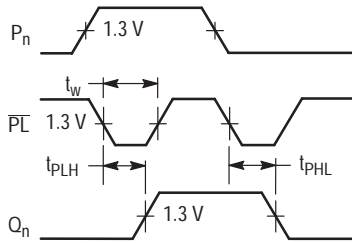


Figure 4.

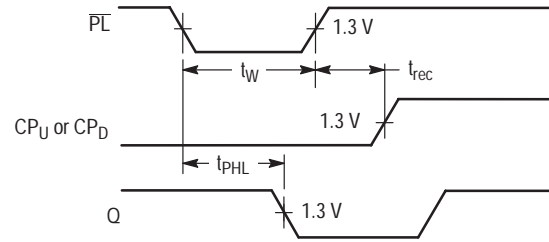
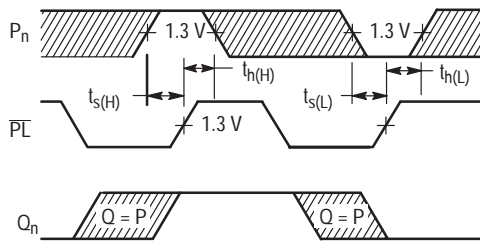


Figure 5.



\* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6.

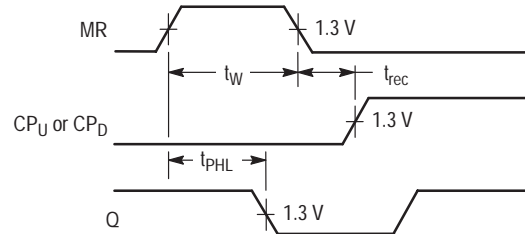


Figure 7.

# SN74LS194A

## 4-Bit Bidirectional Universal Shift Register

The SN74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL families.

- Typical Shift Frequency of 36 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

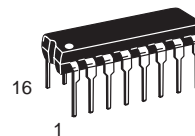
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

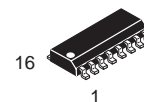


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CASE 648



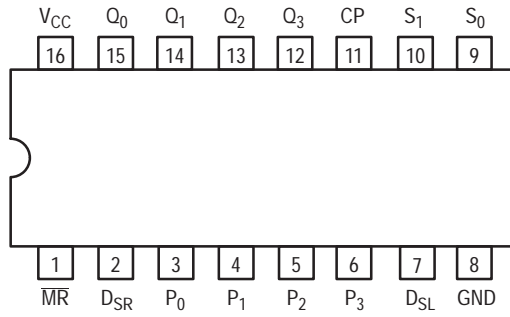
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS194AN	16 Pin DIP	2000 Units/Box
SN74LS194AD	16 Pin	2500/Tape & Reel

# SN74LS194A

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

$S_0, S_1$	Mode Control Inputs
$P_0 - P_3$	Parallel Data Inputs
$D_{SR}$	Serial (Shift Right) Data Input
$D_{SL}$	Serial (Shift Left) Data Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$Q_0 - Q_3$	Parallel Outputs

### LOADING (Note a)

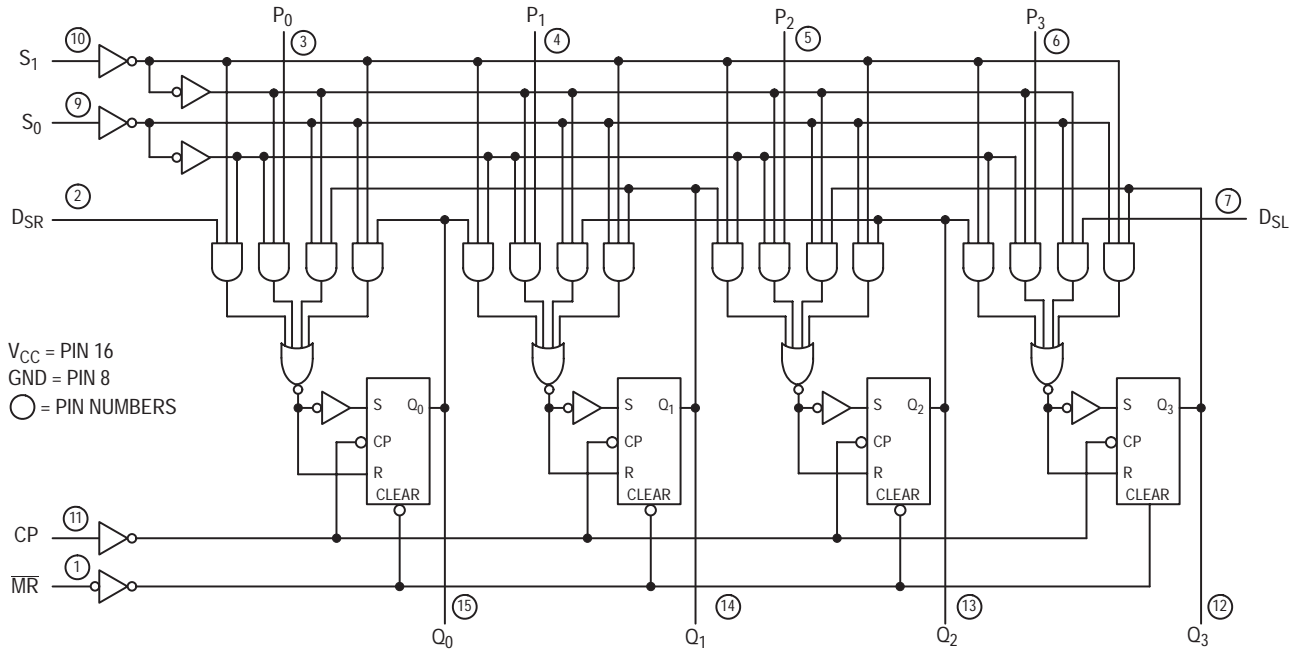
	HIGH	LOW
$S_0, S_1$	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	0.5 U.L.	0.25 U.L.
$D_{SR}$	0.5 U.L.	0.25 U.L.
$D_{SL}$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

# SN74LS194A

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the ON Semiconductor LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

The four parallel data inputs (P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>) are D-type inputs. When both S<sub>0</sub> and S<sub>1</sub> are HIGH, the data appearing on P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, and P<sub>3</sub> inputs is transferred to the Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> outputs respectively following the next LOW to HIGH transition of the clock.

The asynchronous Master Reset ( $\overline{MR}$ ), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

Two mode control inputs (S<sub>0</sub>, S<sub>1</sub>) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, Q<sub>0</sub> → Q<sub>1</sub>, etc.) or right to left (shift left, Q<sub>3</sub> → Q<sub>2</sub>, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S<sub>0</sub> and S<sub>1</sub> are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

D-type serial data inputs (D<sub>SR</sub>, D<sub>SL</sub>) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

# SN74LS194A

## MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	S <sub>1</sub>	S <sub>0</sub>	D <sub>SR</sub>	D <sub>SL</sub>	P <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>
Shift Left	H	h	l	X	l	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	L
	H	h	l	X	h	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	H
Shift Right	H	l	h	l	X	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
	H	l	h	h	X	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
Parallel Load	H	h	h	X	X	P <sub>n</sub>	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

p<sub>n</sub> (q<sub>n</sub>) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			23	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	36		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		14 17	22 26	ns	
t <sub>PHL</sub>	Propagation Delay, MR to Output		19	30	ns	

# SN74LS194A

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock or $\overline{\text{MR}}$ Pulse Width	20			ns	$V_{CC} = 5.0\text{ V}$
$t_s$	Mode Control Setup Time	30			ns	
$t_s$	Data Setup Time	20			ns	
$t_h$	Hold time, Any Input	0			ns	
$t_{\text{rec}}$	Recovery Time	25			ns	

## DEFINITIONS OF TERMS

**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

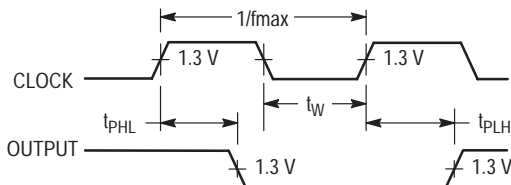
**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME ( $t_{\text{rec}}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

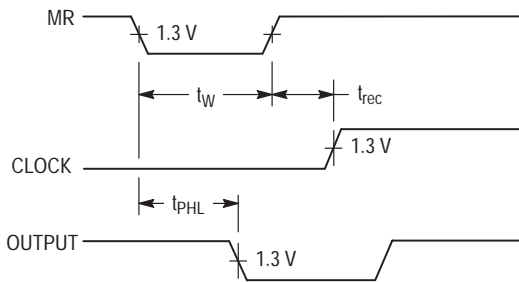
## AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



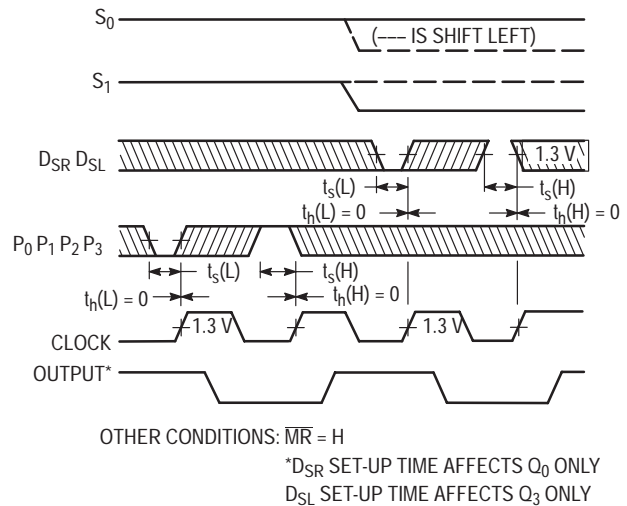
OTHER CONDITIONS:  $S_1 = L, \overline{\text{MR}} = H, S_0 = H$

**Figure 1. Clock to Output Delays Clock Pulse Width and  $f_{\text{max}}$**

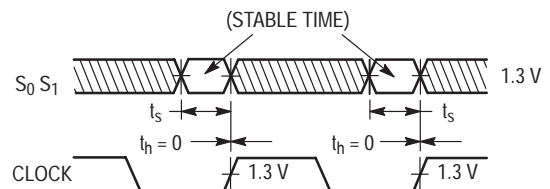


OTHER CONDITIONS:  $S_0, S_1 = H$   
 $P_0 = P_1 = P_2 = P_3 = H$

**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



**Figure 3. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for Serial Data ( $D_{\text{SR}}, D_{\text{SL}}$ ) and Parallel Data ( $P_0, P_1, P_2, P_3$ )**



OTHER CONDITIONS:  $\overline{\text{MR}} = H$

**Figure 4. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for S Input**

# SN74LS195A

## Universal 4-Bit Shift Register

The SN74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL products.

- Typical Shift Right Frequency of 39 MHz
- Asynchronous Master Reset
- J,  $\bar{K}$  Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

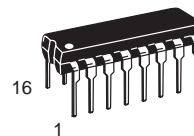
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

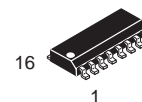


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



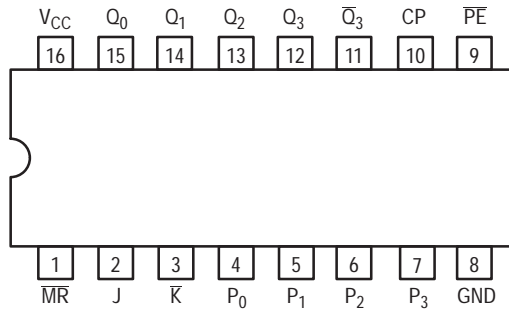
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS195AN	16 Pin DIP	2000 Units/Box
SN74LS195AD	16 Pin	2500/Tape & Reel

# SN74LS195A

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
$P_0 - P_3$	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$Q_0 - Q_3$	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

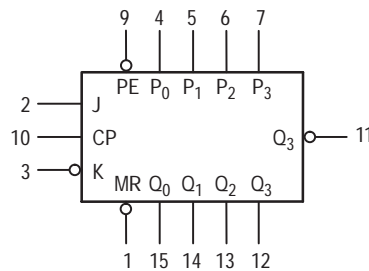
### LOADING (Note a)

	HIGH	LOW
$\overline{PE}$	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	0.5 U.L.	0.25 U.L.
J	0.5 U.L.	0.25 U.L.
$\overline{K}$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
$\overline{Q}_3$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL

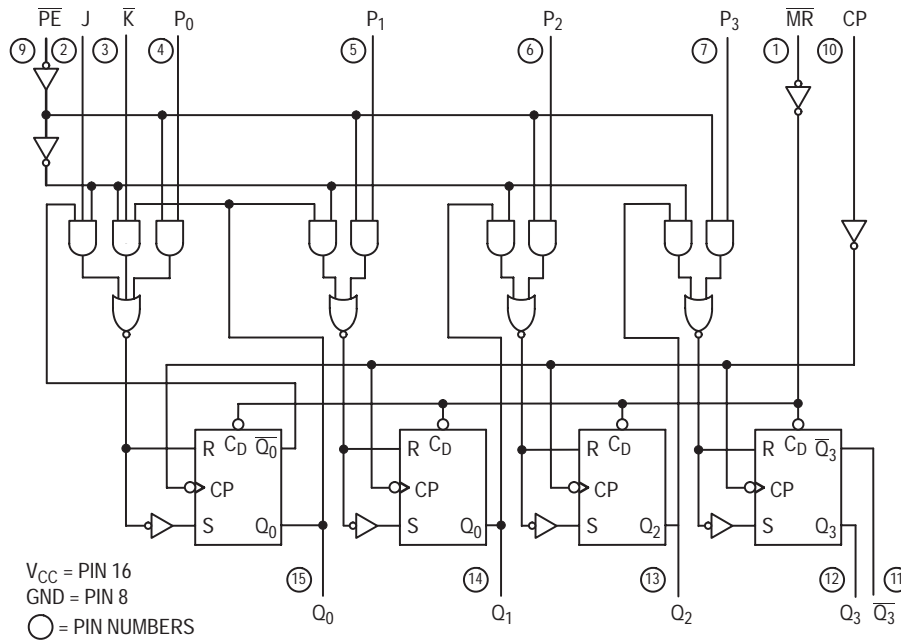


$V_{CC}$  = PIN 16  
GND = PIN 8



# SN74LS195A

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load which are controlled by the state of the Parallel Enable ( $\overline{PE}$ ) input. When the PE input is HIGH, serial data enters the first flip-flop  $Q_0$  via the J and  $\overline{K}$  inputs and is shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$  following each LOW to HIGH clock transition. The  $\overline{JK}$  inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the  $\overline{PE}$

input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs  $P_0, P_1, P_2, P_3$  is transferred to the respective  $Q_0, Q_1, Q_2, Q_3$  outputs following the LOW to HIGH clock transition. Shift left operations ( $Q_3 \rightarrow Q_2$ ) can be achieved by tying the  $Q_n$  Outputs to the  $P_{n-1}$  inputs and holding the  $\overline{PE}$  input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J,  $\overline{K}$ ,  $P_n$  and  $\overline{PE}$  inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ( $\overline{MR}$ ) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Reset First	H	h	l	l	X	L	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	$q_0$	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Parallel Load	H	l	X	X	$p_n$	$p_0$	$p_1$	$p_2$	$p_3$	$\overline{p}_3$

L = LOW voltage levels

H = HIGH voltage levels

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.

$p_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

# SN74LS195A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			21	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	39		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		14 17	22 26	ns	
t <sub>PHL</sub>	Propagation Delay, MR to Output		19	30	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP Clock Pulse Width	16			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	MR Pulse Width	12			ns	
t <sub>s</sub>	PE Setup Time	25			ns	
t <sub>s</sub>	Data Setup Time	15			ns	
t <sub>rec</sub>	Recovery Time	25			ns	
t <sub>rel</sub>	PE Release Time			10	ns	
t <sub>h</sub>	Data Hold Time	0			ns	

**DEFINITIONS OF TERMS**

SETUP TIME( $t_s$ ) —is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

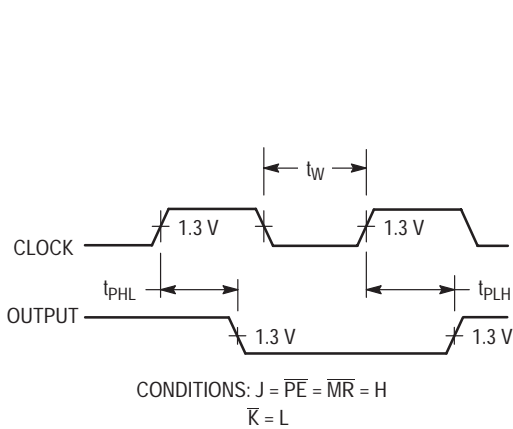
HOLD TIME ( $t_h$ ) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

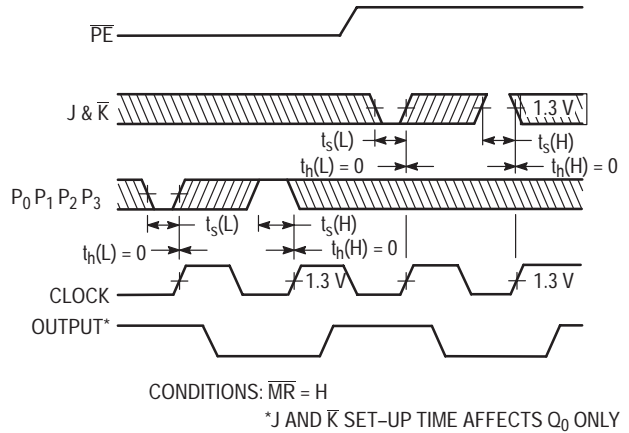
RECOVERY TIME ( $t_{rec}$ ) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

**AC WAVEFORMS**

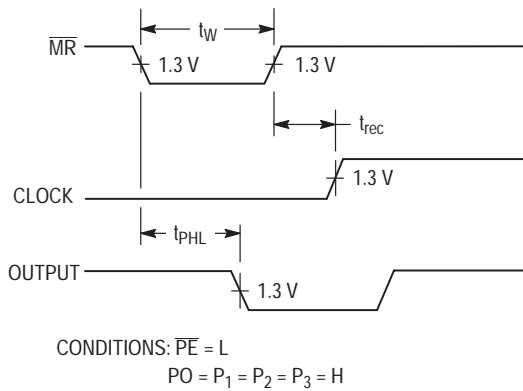
The shaded areas indicate when the input is permitted to change for predictable output performance.



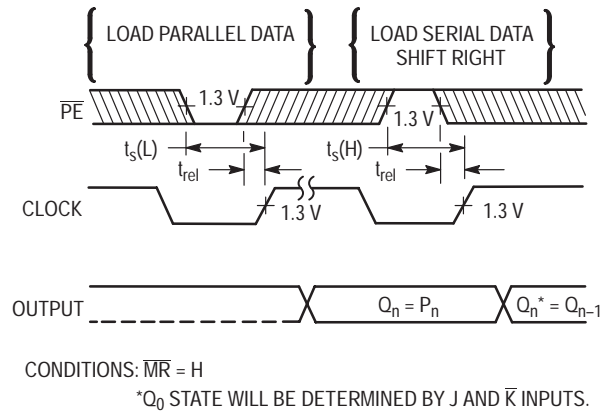
**Figure 1. Clock to Output Delays and Clock Pulse Width**



**Figure 3. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for Serial Data (J &  $\overline{K}$ ) and Parallel Data ( $P_0, P_1, P_2, P_3$ )**



**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



**Figure 4. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for  $\overline{P}$  Input**

# SN74LS221

## Dual Monostable Multivibrators with Schmitt-Trigger Inputs

Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to  $V_{CC}$  noise is also provided by internal latching circuitry.

Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With  $R_{ext} = 2.0 \text{ k}\Omega$  and  $C_{ext} = 0$ , a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of  $V_{CC}$  and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and  $V_{CC}$  ranges for greater than six decades of timing capacitance (10 pF to 10  $\mu\text{F}$ ), and greater than one decade of timing resistance (2.0 to 100  $\text{k}\Omega$  for the SN74LS221). Pulse width is defined by the relationship:  $t_w(\text{out}) = C_{ext}R_{ext} \ln 2.0 \approx 0.7 C_{ext} R_{ext}$ ; where  $t_w$  is in ns if  $C_{ext}$  is in pF and  $R_{ext}$  is in  $\text{k}\Omega$ . If pulse cutoff is not critical, capacitance up to 1000  $\mu\text{F}$  and resistance as low as 1.4  $\text{k}\Omega$  may be used. The range of jitter-free pulse widths is extended if  $V_{CC}$  is 5.0 V and 25°C temperature.

- SN74LS221 is a Dual Highly Stable One-Shot
- Overriding Clear Terminates Output Pulse
- Pin Out is Identical to SN74LS123

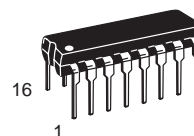
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

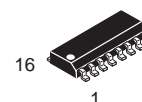


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**LOW  
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**PLASTIC  
N SUFFIX  
CASE 648**



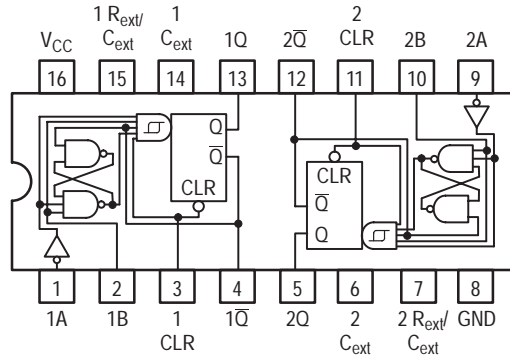
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

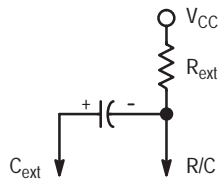
Device	Package	Shipping
SN74LS221N	16 Pin DIP	2000 Units/Box
SN74LS221D	16 Pin	2500/Tape & Reel

# SN74LS221

(TOP VIEW)



Positive logic: Low input to clear resets Q low and  $\bar{Q}$  high regardless of dc levels at A or B inputs.



**FUNCTION TABLE  
(EACH MONOSTABLE)**

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
*↑	L	H		

\*See operational notes — Pulse Trigger Modes

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN74LS221	23 mW	70 s

# SN74LS221

## OPERATIONAL NOTES

Once in the pulse trigger mode, the output pulse width is determined by  $t_W = R_{ext}C_{ext}\ln 2$ , as long as  $R_{ext}$  and  $C_{ext}$  are within their minimum and maximum values and the duty cycle is less than 50%. This pulse width is essentially independent of  $V_{CC}$  and temperature variations. Output pulse widths varies typically no more than  $\pm 0.5\%$  from device to device.

If the duty cycle, defined as being  $100 \cdot \frac{t_W}{T}$  where T is the period of the input pulse, rises above 50%, the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum,  $R_{ext}$  should be as large as possible. (Jitter is independent of  $C_{ext}$ ). With  $R_{ext} = 100K$ , jitter is not appreciable until the duty cycle approaches 90%.

Although the LS221 is pin-for-pin compatible with the LS123, it should be remembered that they are not functionally identical. The LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the LS221. Also note that it is recommended to externally ground the LS123  $C_{ext}$  pin. However, this cannot be done on the LS221.

The SN74LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width,  $t_W$  can be varied over 9 decades of timing by proper selection of the external timing components,  $R_{ext}$  and  $C_{ext}$ .

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers ( $\geq 1.0 \mu V/s$ ). High immunity to  $V_{CC}$  noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard  $V_{CC}$  bypassing is strongly recommended.

The LS221 has four basic modes of operation.

**Clear Mode:** If the clear input is held low, irregardless of the previous output state and other input states, the Q output is low.

**Inhibit Mode:** If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other inputs.

**Pulse Trigger Mode:** A transition of the A or B inputs as indicated in the functional truth table will trigger the Q output to go high for a duration determined by the  $t_W$  equation described above;  $\bar{Q}$  will go low for a corresponding length of time.

The Clear input may also be used to trigger an output pulse, but special logic preconditioning on the A or B inputs must be done as follows:

Following any output triggering action using the A or B inputs, the A input must be set high OR the B input must be set low to allow Clear to be used as a trigger. Inputs should then be set up per the truth table (without triggering the output) to allow Clear to be used a trigger for the output pulse.

If the Clear pin is routinely being used to trigger the output pulse, the A or B inputs must be toggled as described above before and between each Clear trigger event.

Once triggered, as long as the output remains high, all input transitions (except overriding Clear) are ignored.

**Overriding Clear Mode:** If the Q output is high, it may be forced low by bringing the clear input low.

# SN74LS221

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{T+}$	Positive-Going Threshold Voltage at C Input		1.0	2.0	V	$V_{CC} = \text{MIN}$
$V_{T-}$	Negative-Going Threshold Voltage at C Input	0.7	0.8		V	$V_{CC} = \text{MIN}$
$V_{T+}$	Positive-Going Threshold Voltage at B Input		1.0	2.0	V	$V_{CC} = \text{MIN}$
$V_{T-}$	Negative-Going Threshold Voltage at B Input	0.8	0.9		V	$V_{CC} = \text{MIN}$
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for A Input
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for A Input
$V_{IK}$	Input Clamp Voltage			-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.4		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$
$V_{OL}$	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$ , $V_{CC} = \text{MIN}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current Input A Input B Clear			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
				-0.8		
				-0.8		
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current Quiescent		4.7	11	mA	$V_{CC} = \text{MAX}$
	Triggered		19	27		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS221

## AC CHARACTERISTICS ( $V_{CC} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ )

Symbol	From (Input)	To (Output)	Limits			Unit	Test Conditions	
			Min	Typ	Max			
$t_{PLH}$	A	Q		45	70	ns	$C_L = 15\text{ pF}$ , See Figure 1	
	B	Q		35	55			
$t_{PHL}$	A	$\bar{Q}$		50	80	ns		
	B	$\bar{Q}$		40	65			
$t_{PHL}$	Clear	Q		35	55	ns		
$t_{PLH}$	Clear	$\bar{Q}$		44	65	ns		
$t_{W(out)}$	A or B	Q or $\bar{Q}$	70	120	150	ns		$C_{ext} = 80\text{ pF}$ , $R_{ext} = 2.0\ \Omega$
			20	47	70			$C_{ext} = 0$ , $R_{ext} = 2.0\text{ k}\Omega$
			600	670	750			$C_{ext} = 100\text{ pF}$ , $R_{ext} = 10\text{ k}\Omega$
			6.0	6.9	7.5			ms

## AC SETUP REQUIREMENTS ( $V_{CC} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$dv/dt$	Rate of Rise or Fall of Input Pulse	Schmitt, B	1.0		V/s
		Logic Input, A	1.0		V/ $\mu\text{s}$
$t_W$	Input Pulse Width	A or B, $t_{W(in)}$	40		ns
		Clear, $t_W(\text{clear})$	40		
$t_s$	Clear-Inactive-State Setup Time	15		ns	
$R_{ext}$	External Timing Resistance	1.4		100	$\text{k}\Omega$
$C_{ext}$	External Timing Capacitance	0		1000	$\mu\text{F}$
	Output Duty Cycle	$R_T = 2.0\text{ k}\Omega$		50	%
		$R_T = \text{MAX } R_{ext}$		90	



# SN74LS221

## AC WAVEFORMS

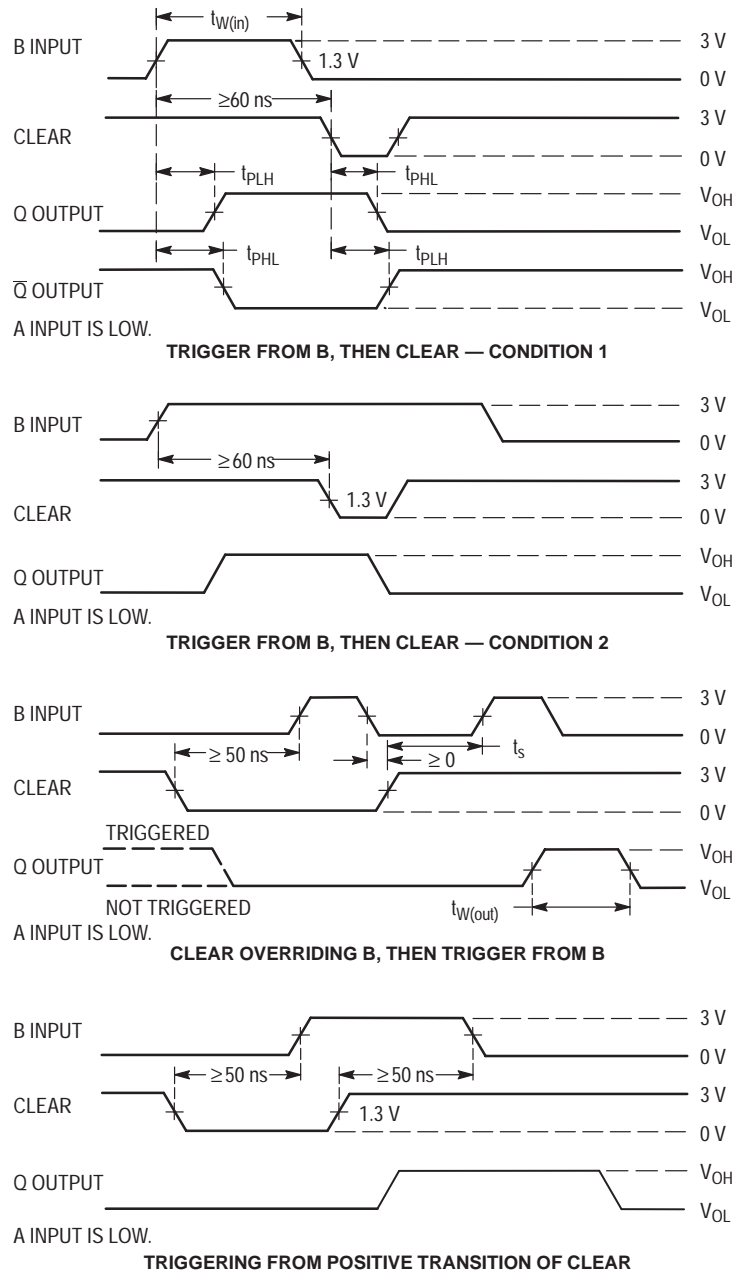


Figure 1.

# SN74LS240 SN74LS244

## Octal Buffer/Line Driver with 3-State Outputs

The SN74LS240 and SN74LS244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

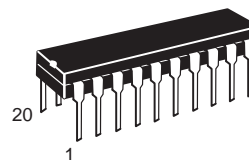
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–3.0	mA
				–15	mA
I <sub>OL</sub>	Output Current – Low			24	mA

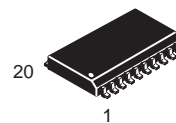


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SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 738**



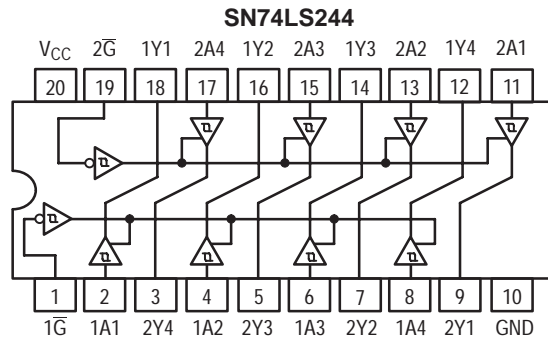
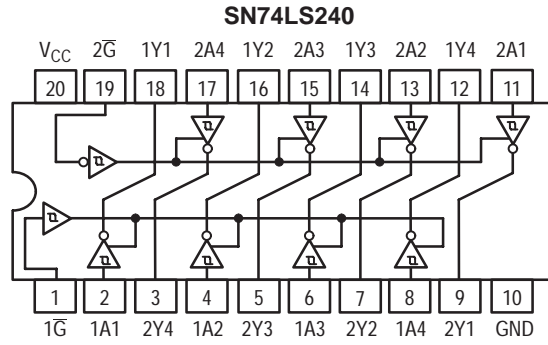
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS240N	16 Pin DIP	1440 Units/Box
SN74LS240DW	16 Pin	2500/Tape & Reel
SN74LS244N	16 Pin DIP	1440 Units/Box
SN74LS244DW	16 Pin	2500/Tape & Reel

# SN74LS240 SN74LS244

## LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



## TRUTH TABLES

**SN74LS240**

INPUTS		OUTPUT
$1\bar{G}, 2\bar{G}$	D	
L	L	H
L	H	L
H	X	(Z)

**SN74LS244**

INPUTS		OUTPUT
$1\bar{G}, 2\bar{G}$	D	
L	L	L
L	H	H
H	X	(Z)

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance

# SN74LS240 SN74LS244

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	0.2	0.4		V	V <sub>CC</sub> = MIN
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -3.0 mA
		2.0			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Output Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			27	mA	V <sub>CC</sub> = MAX
	Total, Output LOW	LS240		44		
		LS244		46		
	Total at HIGH Z	LS240		50		
		LS244		54		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output LS244		12 12	18 18	ns	
t <sub>PZH</sub>	Output Enable Time to HIGH Level		15	23	ns	
t <sub>PZL</sub>	Output Enable Time to LOW Level		20	30	ns	
t <sub>PLZ</sub>	Output Disable Time from LOW Level		15	25	ns	C <sub>L</sub> = 5.0 pF, R <sub>L</sub> = 667 Ω
t <sub>PHZ</sub>	Output Disable Time from HIGH Level		10	18	ns	

# SN74LS240 SN74LS244

## AC WAVEFORMS

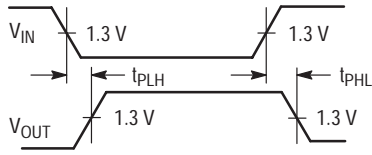


Figure 1.

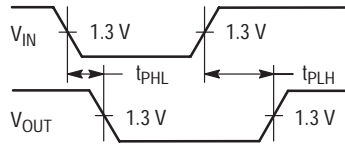


Figure 2.

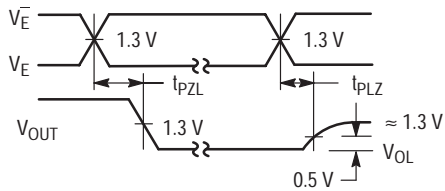


Figure 3.

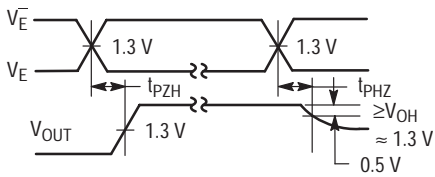
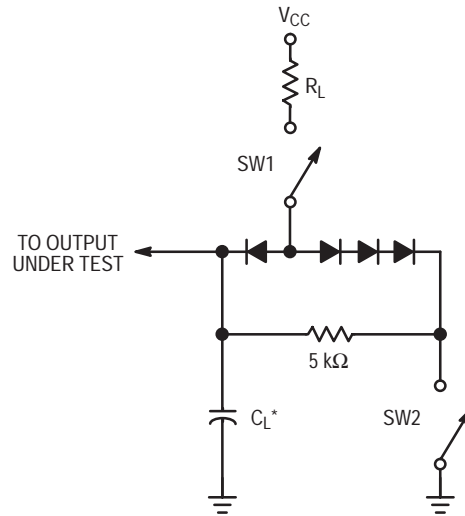


Figure 4.



SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

Figure 5.

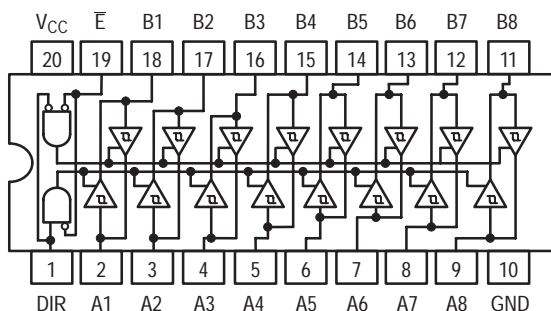
# SN74LS245

## Octal Bus Transceiver

The SN74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ( $\bar{E}$ ) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

### LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



### TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

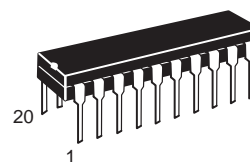
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-3.0	mA
				-15	mA
$I_{OL}$	Output Current – Low			24	mA

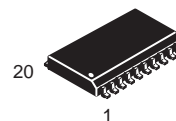


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 738**



**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS245N	16 Pin DIP	1440 Units/Box
SN74LS245DW	16 Pin	2500/Tape & Reel

# SN74LS245

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	0.2	0.4		V	V <sub>CC</sub> = MIN
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -3.0 mA
		2.0			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-200	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current	A or B, DR or E		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		DR or E		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
		A or B		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 5.5 V
I <sub>IL</sub>	Input LOW Current			-0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Output Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			70	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.



## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V, T<sub>RISE</sub>/T<sub>FALL</sub> ≤ 6.0 ns)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PZH</sub>	Output Enable Time to HIGH Level		25	40		
t <sub>PZL</sub>	Output Enable Time to LOW Level		27	40		
t <sub>PLZ</sub>	Output Disable Time from LOW Level		15	25	ns	C <sub>L</sub> = 5.0 pF, R <sub>L</sub> = 667 Ω
t <sub>PHZ</sub>	Output Disable Time from HIGH Level		15	25		

# SN74LS247

## BCD-to-Seven-Segment Decoders/Drivers

The SN74LS247 is a BCD-to-Seven-Segment Decoder/Drivers.

The LS247 composes the  and  with the tails. The LS247 has active-low outputs for direct drive of indicators.

The LS247 features a lamp test input and have full ripple-blanking input/output controls. An automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High BI/RBO			-50	$\mu$ A
$I_{OL}$	Output Current – Low BI/RBO			3.2	mA
$V_{O(off)}$	Off-State Output Voltage a – g			15	V
$I_{O(on)}$	On-State Output Current a – g			24	mA

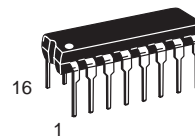


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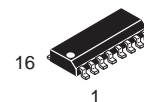
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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648



SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

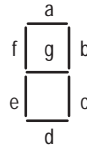
Device	Package	Shipping
SN74LS247N	16 Pin DIP	2000 Units/Box
SN74LS247D	16 Pin	2500/Tape & Reel



# SN74LS247

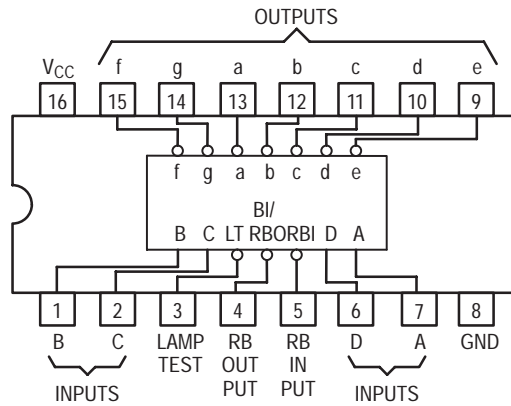


**NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS**



**SEGMENT IDENTIFICATION**

**SN74LS247  
(TOP VIEW)**



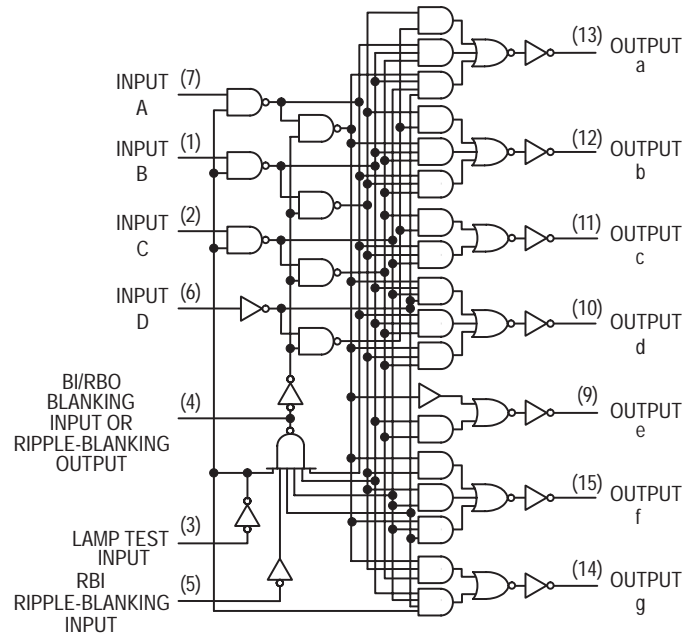
**CIRCUIT FEATURES LAMP INTENSITY MODULATION CAPABILITY**

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
SN74LS247	low	open-collector	24 mA	15 V	35 mW

# SN74LS247

## LOGIC DIAGRAM

### LS247



# SN74LS247

## LS247 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO <sup>†</sup>	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = HIGH Level, L = LOW Level, X = Irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

<sup>†</sup> BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

# SN74LS247

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage BI/RBO	2.4	4.2		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage BI/RBO		0.25	0.4	V	$I_{OL} = 1.6 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{O(\text{off})}$	Off-State Output Current a-g			250	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IH} = 2.0 \text{ V}$ , $V_{O(\text{off})} = 15 \text{ V}$ , $V_{IL} = \text{MAX}$
$V_{O(\text{on})}$	On-State Output Voltage a-g		0.25	0.4	V	$I_{O(\text{on})} = 12 \text{ mA}$ $V_{CC} = \text{MIN}$ , $V_{IH} = 2.0 \text{ V}$ , $V_{IL}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current Any Input, except BI/RBO BI/RBO			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
				-1.2		
$I_{OS}$	Short Circuit Current BI/RBO (Note 1)	-0.3		-2.0	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current		7.0	13	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V}$ , $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Turn-Off Time from A Input Turn-On Time from A Input			100 100	ns	$C_L = 15 \text{ pF}$ , $R_L = 665 \Omega$
$t_{PHL}$ $t_{PLH}$	Turn-Off Time from RBI Input Turn-On Time from RBI Input			100 100	ns	

# SN74LS251

## 8-Input Multiplexer with 3-State Outputs

The TTL/MSI SN74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Inverting and Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

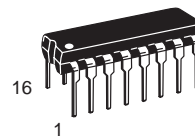
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-2.6	mA
I <sub>OL</sub>	Output Current – Low			24	mA

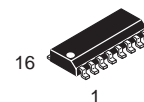


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



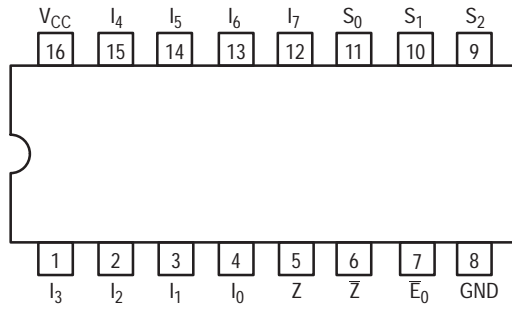
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS251N	16 Pin DIP	2000 Units/Box
SN74LS251D	16 Pin	2500/Tape & Reel

# SN74LS251

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

$S_0 - S_2$	Select Inputs
$\bar{E}_0$	Output Enable (Active LOW) Inputs
$I_0 - I_7$	Multiplexer Inputs
Z	Multiplexer Output
$\bar{Z}$	Complementary Multiplexer Output

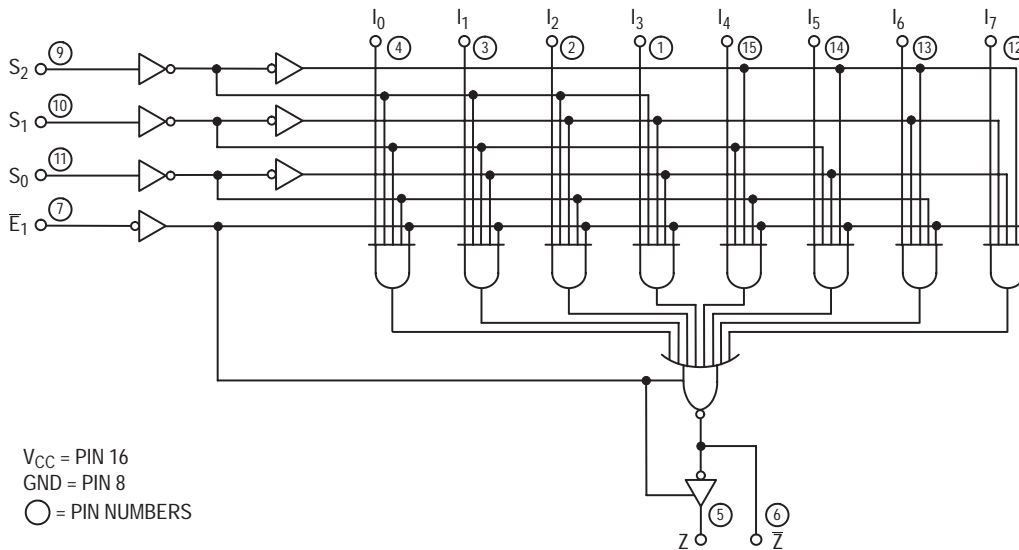
### LOADING (Note a)

	HIGH	LOW
$S_0 - S_2$	0.5 U.L.	0.25 U.L.
$\bar{E}_0$	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	0.5 U.L.	0.25 U.L.
Z	65 U.L.	15 U.L.
$\bar{Z}$	65 U.L.	15 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

## LOGIC DIAGRAM



# SN74LS251

## FUNCTIONAL DESCRIPTION

The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Output Enable input ( $\bar{E}_O$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \bar{E}_O \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltage.

TRUTH TABLE

$\bar{E}_O$	$S_2$	$S_1$	$S_0$	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
(Z) = High impedance (Off)

# SN74LS251

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			10	mA	V <sub>CC</sub> = MAX, V <sub>E</sub> = 0 V
				12	mA	V <sub>CC</sub> = MAX, V <sub>E</sub> = 4.5 V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Z Output		20 21	33 33	ns	Figure 1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Z Output		29 28	45 45	ns	Figure 2
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Z̄ Output		10 9.0	15 15	ns	Figure 1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Z Output		17 18	28 28	ns	Figures 2
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to Z̄ Output		17 24	27 40	ns	Figures 4, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to Z Output		30 26	45 40	ns	Figures 3, 5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time to Z̄ Output		37 15	55 25	ns	Figures 3, 5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time to Z Output		30 15	45 25	ns	Figures 4, 5

C<sub>L</sub> = 15 pF,  
R<sub>L</sub> = 2.0 kΩ

C<sub>L</sub> = 5.0 pF,  
R<sub>L</sub> = 667 kΩ



# SN74LS251

## 3-STATE AC WAVEFORMS

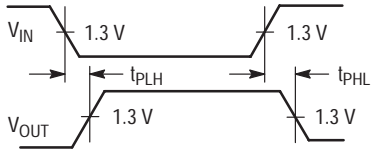


Figure 1.

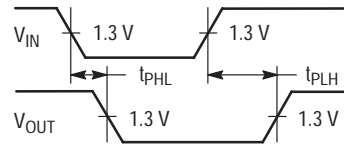


Figure 2.

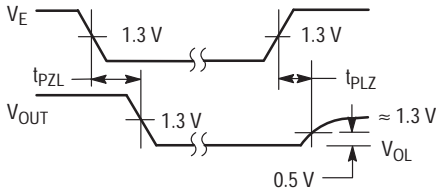


Figure 3.

0.5 V

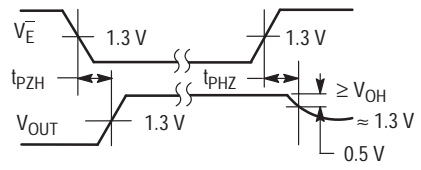
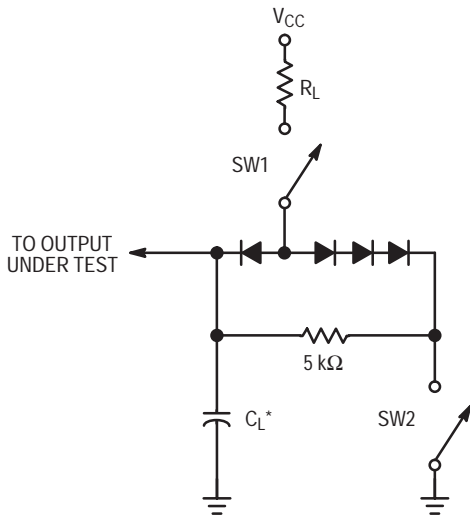


Figure 4.

## AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

Figure 5.

# SN74LS253

## Dual 4-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ( $\bar{E}_0$ ) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

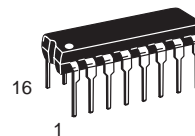
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-2.6	mA
I <sub>OL</sub>	Output Current – Low			24	mA

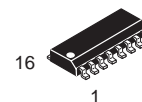


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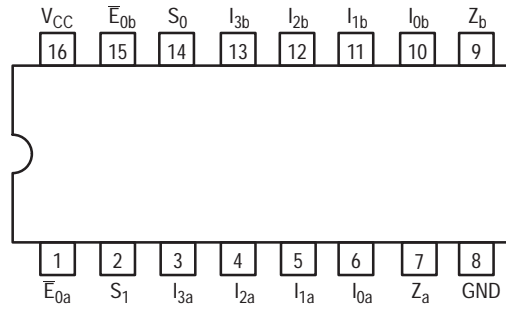
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS253N	16 Pin DIP	2000 Units/Box
SN74LS253D	16 Pin	2500/Tape & Reel

# SN74LS253

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$S_0, S_1$	Common Select Inputs
<b>Multiplexer A</b>	
$\bar{E}_{0a}$	Output Enable (Active LOW) Input
$I_{0a} - I_{3a}$	Multiplexer Inputs
$Z_a$	Multiplexer Output
<b>Multiplexer B</b>	
$\bar{E}_{0b}$	Output Enable (Active LOW) Input
$I_{0b} - I_{3b}$	Multiplexer Inputs
$Z_b$	Multiplexer Output

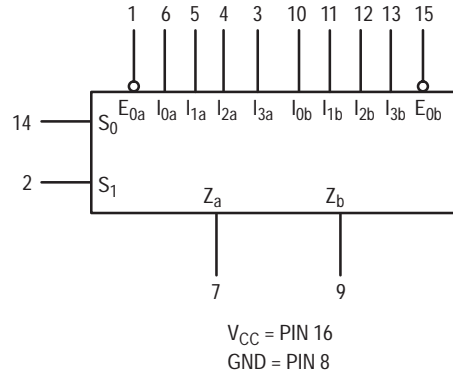
### LOADING (Note a)

	HIGH	LOW
$S_0, S_1$	0.5 U.L.	0.25 U.L.
$\bar{E}_{0a}$	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	0.5 U.L.	0.25 U.L.
$Z_a$	65 U.L.	15 U.L.
$\bar{E}_{0b}$	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	0.5 U.L.	0.25 U.L.
$Z_b$	65 U.L.	15 U.L.

### NOTES:

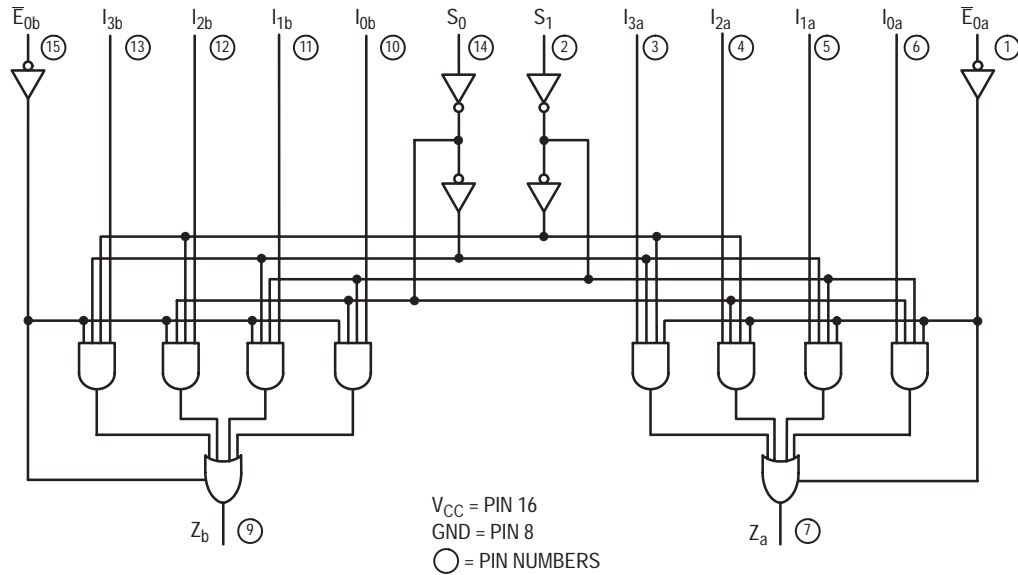
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



# SN74LS253

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs ( $S_0$ ,  $S_1$ ). The 4-input multiplexers have individual Output Enable ( $\bar{E}_{0a}$ ,  $\bar{E}_{0b}$ ) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

### TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
$S_0$	$S_1$	$I_0$	$I_1$	$I_2$	$I_3$	$\bar{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level

L = LOW Level

X = Irrelevant

(Z) = High Impedance (off)

Address inputs  $S_0$  and  $S_1$  are common to both sections.

# SN74LS253

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V		
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			12	mA	V <sub>CC</sub> = MAX, V <sub>E</sub> = 0 V	
				14	mA	V <sub>CC</sub> = MAX, V <sub>E</sub> = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V) See SN74LS251 for Waveforms

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		17 13	25 20	ns	Figure 1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Output		30 21	45 32	ns	Figure 1
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		15 15	28 23	ns	Figures 4, 5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		27 18	41 27	ns	Figures 3, 5

C<sub>L</sub> = 45 pF,  
R<sub>L</sub> = 667 Ω

C<sub>L</sub> = 5.0 pF,  
R<sub>L</sub> = 667 Ω

# SN74LS257B SN74LS258B

## Quad 2-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS257B and the SN74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ( $E_O$ ) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

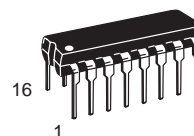
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-2.6	mA
$I_{OL}$	Output Current – Low			24	mA

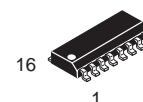


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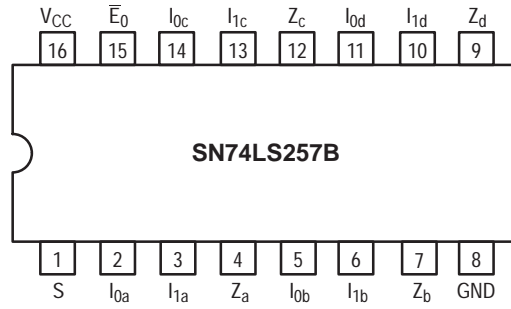
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

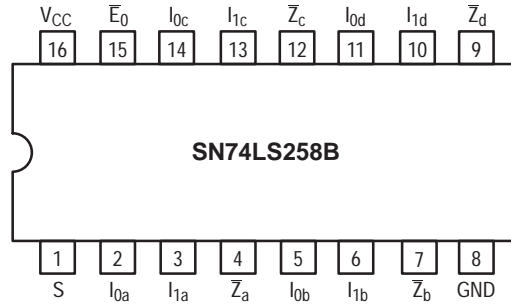
Device	Package	Shipping
SN74LS257BN	16 Pin DIP	2000 Units/Box
SN74LS257BD	16 Pin	2500/Tape & Reel
SN74LS258BN	16 Pin DIP	2000 Units/Box
SN74LS258BD	16 Pin	2500/Tape & Reel

# SN74LS257B SN74LS258B

## CONNECTION DIAGRAM DIP (TOP VIEW)



V<sub>CC</sub> = PIN 16  
GND = PIN 8

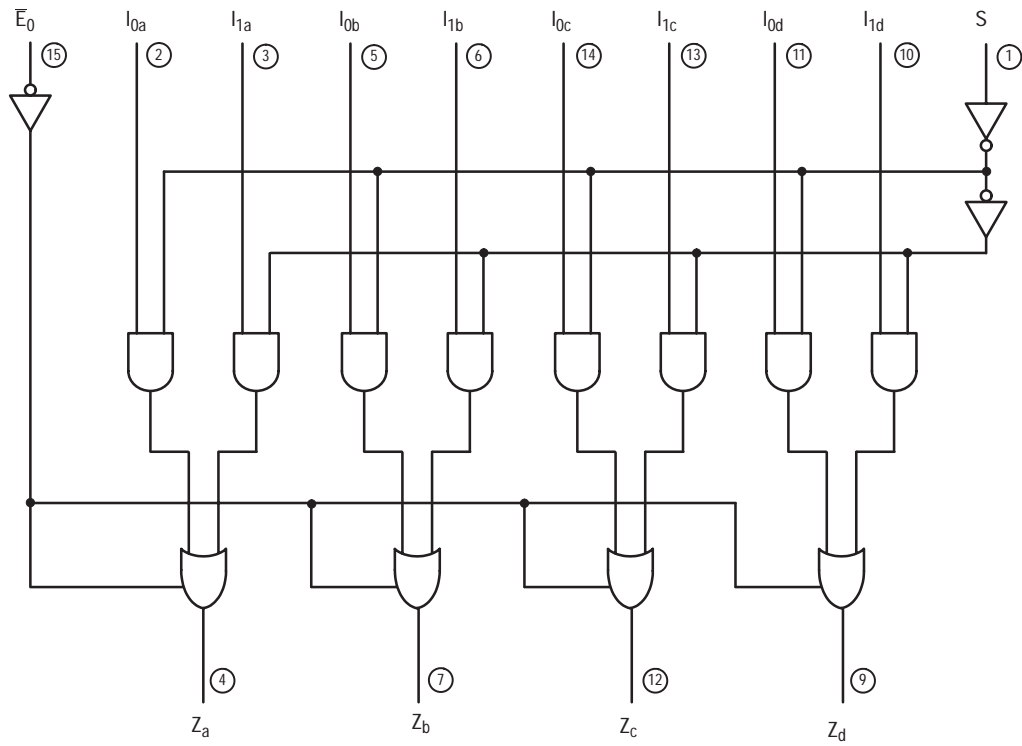


NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

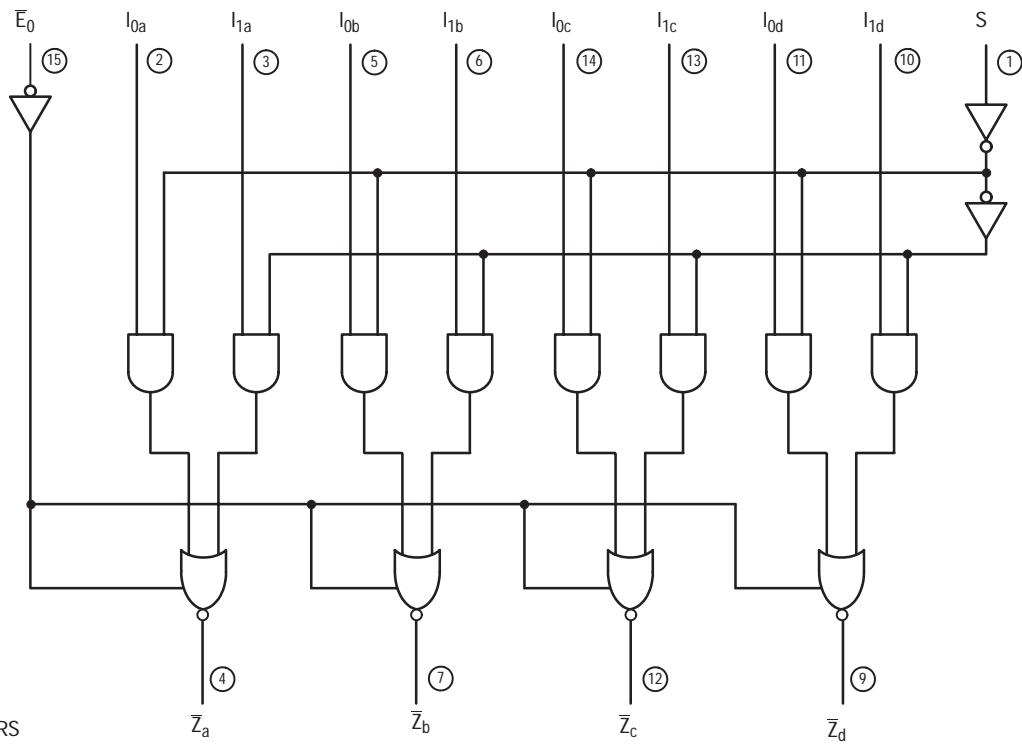
# SN74LS257B SN74LS258B

## LOGIC DIAGRAMS

### SN74LS257B



### SN74LS258B



$V_{CC}$  = PIN 16  
GND = PIN 8  
○ = PIN NUMBERS



## SN74LS257B SN74LS258B

### FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I<sub>0</sub> inputs are selected and when Select is HIGH, the I<sub>1</sub> inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

#### LS257B

$$\begin{aligned} Z_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Z_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= \bar{E}_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Z_d &= \bar{E}_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

When the Output Enable Input ( $\bar{E}_0$ ) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

#### LS258B

$$\begin{aligned} \bar{Z}_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Z}_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Z}_c &= \bar{E}_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Z}_d &= \bar{E}_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257B	OUTPUTS LS258B
$\bar{E}_0$	S	I <sub>0</sub>	I <sub>1</sub>	Z	$\bar{Z}$
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 (Z) = High Impedance (off)

# SN74LS257B SN74LS258B

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>OZH</sub>	Output Off Current — HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current — LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current Other Inputs S Inputs			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Other Inputs S Inputs			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current All Inputs			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH	LS257B LS258B		10 9.0	mA	V <sub>CC</sub> = MAX
	Total, Output LOW	LS257B LS258B		16 14	mA	
	Total, Output 3-State	LS257B LS258B		19 16	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V) See SN74LS251 for Waveforms

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		10 12	13 15	ns	Figures 1 & 2	C <sub>L</sub> = 45 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Output		14 14	21 21	ns	Figures 1 & 2	
t <sub>PZH</sub>	Output Enable Time to HIGH Level		20	25	ns	Figures 4 & 5	C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PZL</sub>	Output Enable Time to LOW Level		20	25	ns	Figures 3 & 5	
t <sub>PLZ</sub>	Output Disable Time to LOW Level		16	25	ns	Figures 3 & 5	C <sub>L</sub> = 5.0 pF R <sub>L</sub> = 667 Ω
t <sub>PHZ</sub>	Output Disable Time from HIGH Level		18	25	ns	Figures 4 & 5	

# SN74LS259

## 8-Bit Addressable Latch

The SN74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

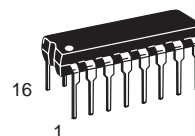
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

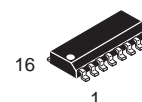


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**PLASTIC  
N SUFFIX  
CASE 648**



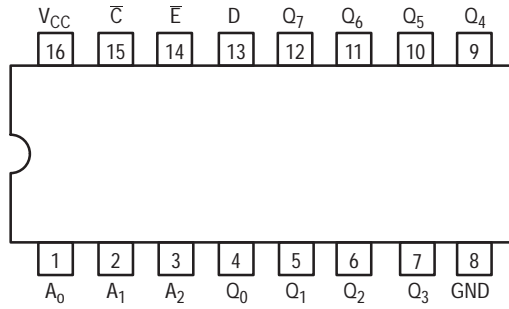
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS259N	16 Pin DIP	2000 Units/Box
SN74LS259D	16 Pin	2500/Tape & Reel

# SN74LS259

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

$A_0, A_1, A_2$	Address Inputs
D	Data Input
$\bar{E}$	Enable (Active LOW) Input
$\bar{C}$	Clear (Active LOW) Input
$Q_0 - Q_7$	Parallel Latch Outputs

### LOADING (Note a)

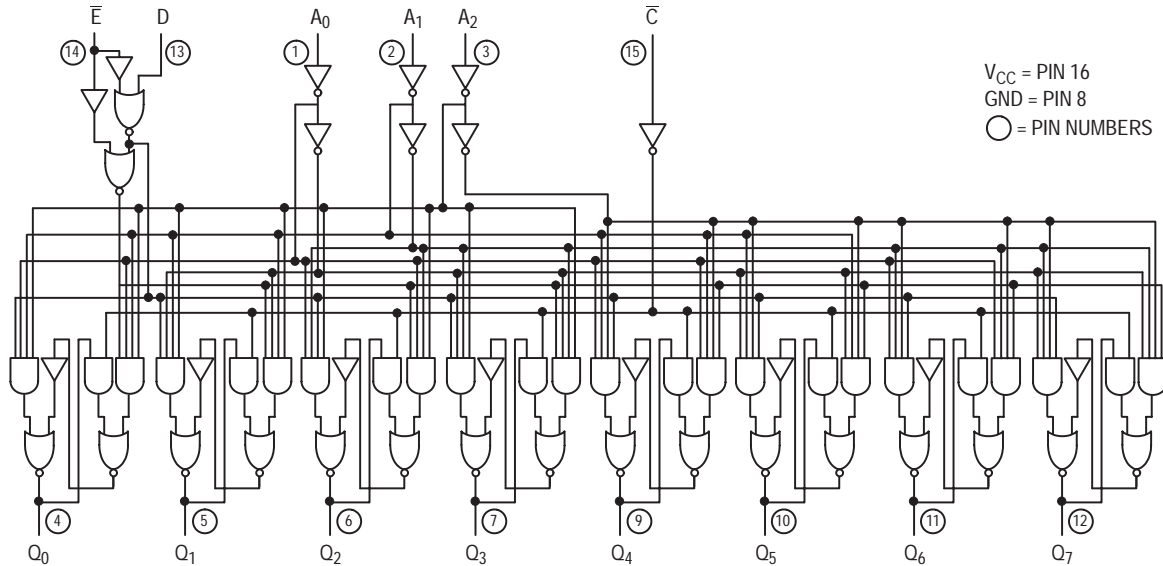
	HIGH	LOW
$A_0, A_1, A_2$	0.5 U.L.	0.25 U.L.
D	0.5 U.L.	0.25 U.L.
$\bar{E}$	1.0 U.L.	0.5 U.L.
$\bar{C}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

# SN74LS259

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The SN74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all

other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

### MODE SELECTION

E	C̄	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

### TRUTH TABLE

#### PRESENT OUTPUT STATES

C̄	E	D	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	MODE		
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear Demultiplex		
L	L	H	L	L	L	H	L	L	L	L	L	L	L			
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Memory		
L	L	H	H	L	L	L	H	L	L	L	L	L	L			
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Addressable Latch		
H	H	X	X	X	X	$Q_{N-1}$	→									
H	L	L	H	L	L	L	$Q_{N-1}$	$Q_{N-1}$	$Q_{N-1}$	→				Addressable Latch		
H	L	H	L	L	L	H	$Q_{N-1}$	$Q_{N-1}$	$Q_{N-1}$	→						
H	L	L	H	L	L	$Q_{N-1}$	L	$Q_{N-1}$	→							
H	L	H	H	L	L	$Q_{N-1}$	H	$Q_{N-1}$	→							
•	•	•	•	•	•									Addressable Latch		
•	•	•	•	•	•											
•	•	•	•	•	•											
•	•	•	•	•	•											
H	L	L	H	H	H	$Q_{N-1}$	→							$Q_{N-1}$	L	Addressable Latch
H	L	H	H	H	H	$Q_{N-1}$	→							$Q_{N-1}$	H	

X = Don't Care Condition  
 L = LOW Voltage Level  
 H = HIGH Voltage Level  
 $Q_{N-1}$  = Previous Output State

# SN74LS259

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			36	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

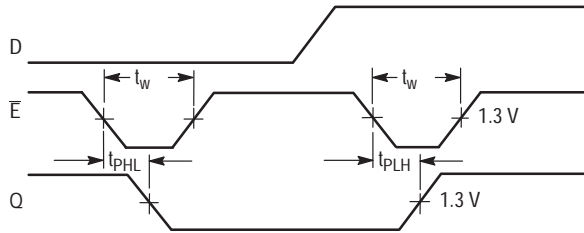
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		22 15	35 24	ns ns	C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	32 21	ns ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		24 18	38 29	ns ns	
t <sub>PHL</sub>	Turn-On Delay, Clear to Output		17	27	ns	

## AC SET-UP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

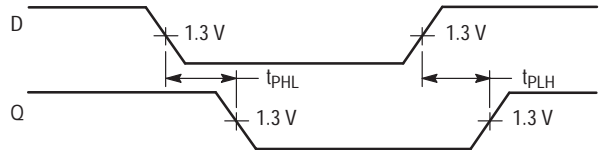
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t <sub>s</sub>	Input Setup Time	20			ns
t <sub>w</sub>	Pulse Width, Clear or Enable	15			ns
t <sub>h</sub>	Hold Time, Data	5.0			ns
t <sub>h</sub>	Hold Time, Address	20			ns

AC WAVEFORMS



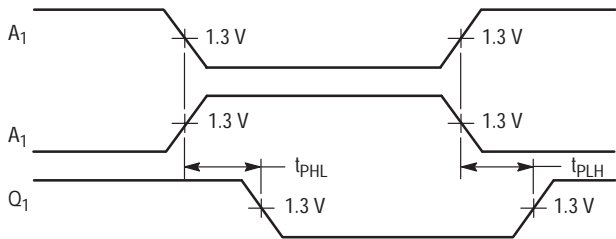
OTHER CONDITIONS:  $\bar{C} = H, A = \text{STABLE}$

**Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width**



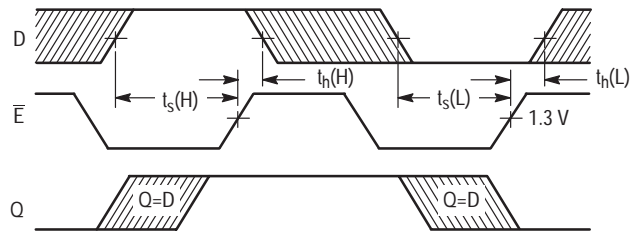
OTHER CONDITIONS:  $\bar{E} = L, \bar{C} = H, A = \text{STABLE}$

**Figure 2. Turn-on and Turn-off Delays, Data to Output**



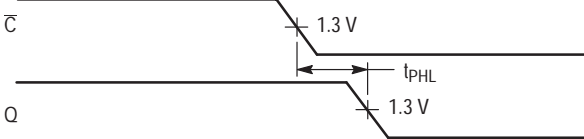
OTHER CONDITIONS:  $\bar{E} = L, \bar{C} = L, D = H$

**Figure 3. Turn-on and Turn-off Delays, Address to Output**



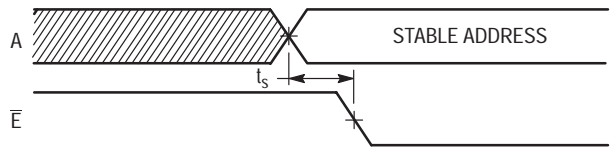
OTHER CONDITIONS:  $\bar{C} = H, A = \text{STABLE}$

**Figure 4. Setup and Hold Time, Data to Enable**



OTHER CONDITIONS:  $\bar{E} = H$

**Figure 5. Turn-on Delay, Clear to Output**



OTHER CONDITIONS:  $\bar{C} = H$

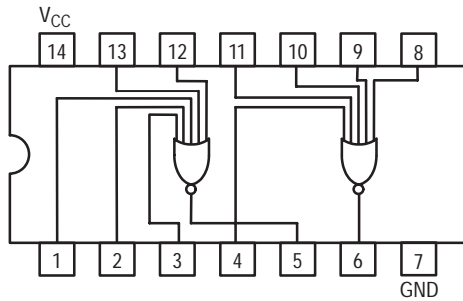
**Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)**

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

# SN74LS260

## Dual 5-Input NOR Gate

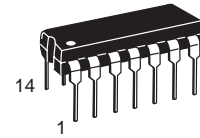


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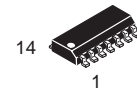
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA



**PLASTIC  
N SUFFIX  
CASE 646**



**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS260N	14 Pin DIP	2000 Units/Box
SN74LS260D	14 Pin	2500/Tape & Reel



# SN74LS260

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			4.0	mA	V <sub>CC</sub> = MAX
				5.5		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub>	Turn-Off Delay, Input to Output		5.0	15	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Turn-On Delay, Input to Output		6.0	15	ns	

# SN74LS273

## Octal D Flip-Flop with Clear

The SN74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

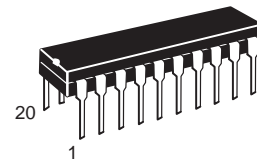
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

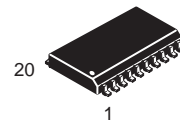


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**LOW  
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CASE 738**



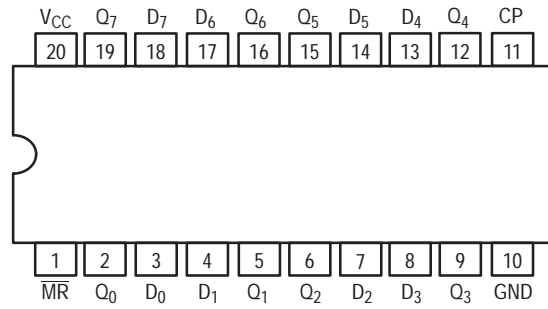
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS273N	16 Pin DIP	1440 Units/Box
SN74LS273DW	16 Pin	2500/Tape & Reel

# SN74LS273

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

CP	Clock (Active HIGH Going Edge) Input
$D_0 - D_7$	Data Inputs
$\overline{MR}$	Master Reset (Active LOW) Input
$Q_0 - Q_7$	Register Outputs

### LOADING (Note a)

	HIGH	LOW
CP	0.5 U.L.	0.25 U.L.
$D_0 - D_7$	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	10 U.L.	5 U.L.

### NOTES:

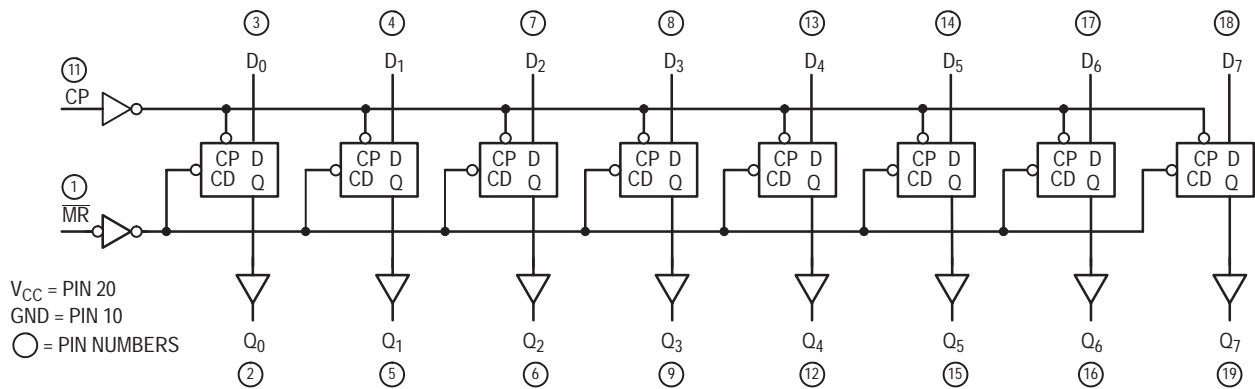
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### TRUTH TABLE

$\overline{MR}$	CP	$D_x$	$Q_x$
L	X	X	L
H		H	H
H		L	L

H = HIGH Logic Level  
L = LOW Logic Level  
X = Immaterial

### LOGIC DIAGRAM



# SN74LS273

## FUNCTIONAL DESCRIPTION

The SN74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the  $\overline{MR}$  input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the

setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			27	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

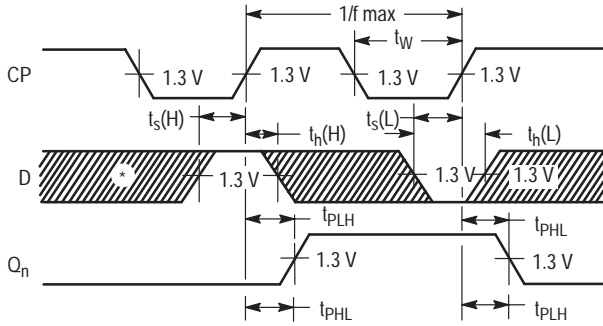
## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Input Clock Frequency	30	40		MHz	Figure 1
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to Q Output		18	27	ns	Figure 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Clock to Output		17 18	27 27	ns	Figure 1

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_w$	Pulse Width, Clock or Clear	20			ns	Figure 1
$t_s$	Data Setup Time	20			ns	Figure 1
$t_h$	Hold Time	5.0			ns	Figure 1
$t_{rec}$	Recovery Time	25			ns	Figure 2

AC WAVEFORMS



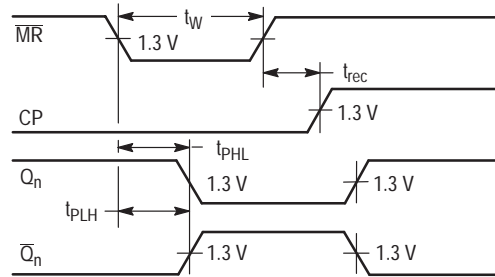
\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**

**DEFINITION OF TERMS**

**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

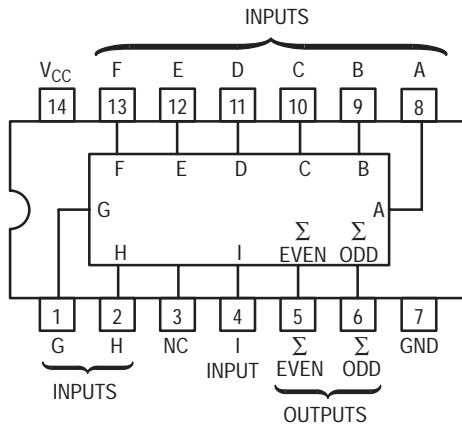
# SN74LS280

## 9-Bit Odd/Even Parity Generators/Checkers

The SN74LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at Pin 4 and the absence of any connection at Pin 3. This design permits the LS280 to be substituted for the LS180 which results in improved performance. The LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- Generates Either Odd or Even Parity for Nine Data Lines
- Typical Data-to-Output Delay of only 33 ns
- Cascadable for n-Bits
- Can Be Used To Upgrade Systems Using MSI Parity Circuits
- Typical Power Dissipation = 80 mW



FUNCTION TABLE

NUMBER OF INPUTS A THRU 1 THAT ARE HIGH	OUTPUTS	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Level, L = LOW Level

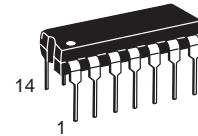
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

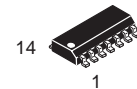


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**PLASTIC  
N SUFFIX  
CASE 646**



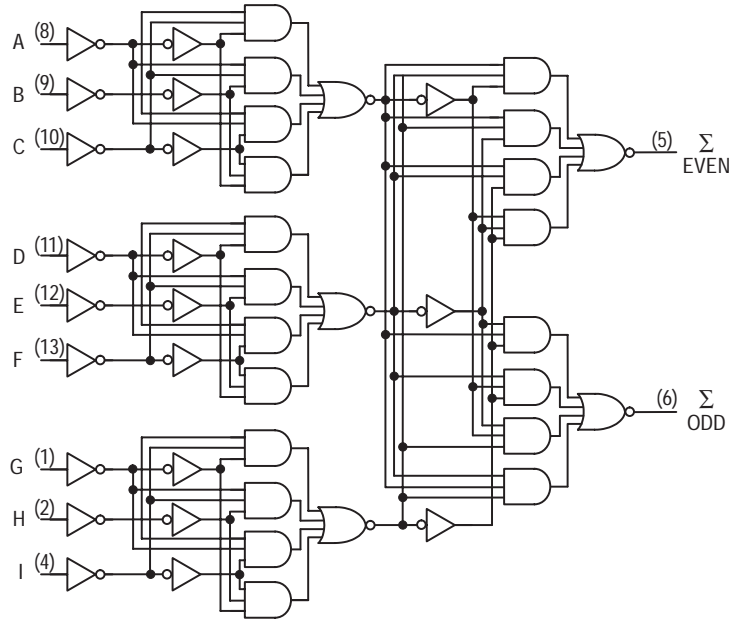
**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS280N	14 Pin DIP	2000 Units/Box
SN74LS280D	14 Pin	2500/Tape & Reel

# SN74LS280

## FUNCTIONAL BLOCK DIAGRAM



### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$	
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$	
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$	
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
$I_{CC}$	Power Supply Current			27	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

### AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Data to Output $\Sigma\text{EVEN}$		33 29	50 45	ns	$C_L = 15 \text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Data to Output $\Sigma\text{ODD}$		23 31	35 50	ns	

# SN74LS283

## 4-Bit Binary Full Adder with Fast Carry

The SN74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ( $A_1$ – $A_4$ ,  $B_1$ – $B_4$ ) and a Carry Input ( $C_0$ ). It generates the binary Sum outputs ( $\Sigma_1$ – $\Sigma_4$ ) and the Carry Output ( $C_4$ ) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			–0.4	mA
$I_{OL}$	Output Current – Low			8.0	mA

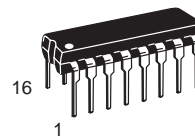


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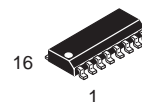
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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648



SOIC  
D SUFFIX  
CASE 751B

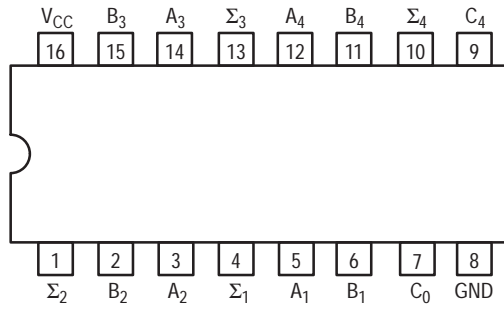
### ORDERING INFORMATION

Device	Package	Shipping
SN74LS283N	16 Pin DIP	2000 Units/Box
SN74LS283D	16 Pin	2500/Tape & Reel



# SN74LS283

## CONNECTION DIAGRAM DIP (TOP VIEW)



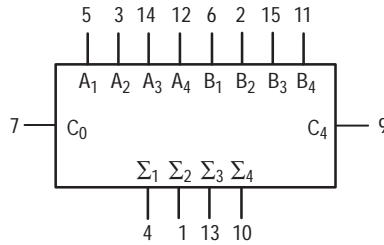
NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
$C_0$	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs	10 U.L.	5 U.L.
$C_4$	Carry Output	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

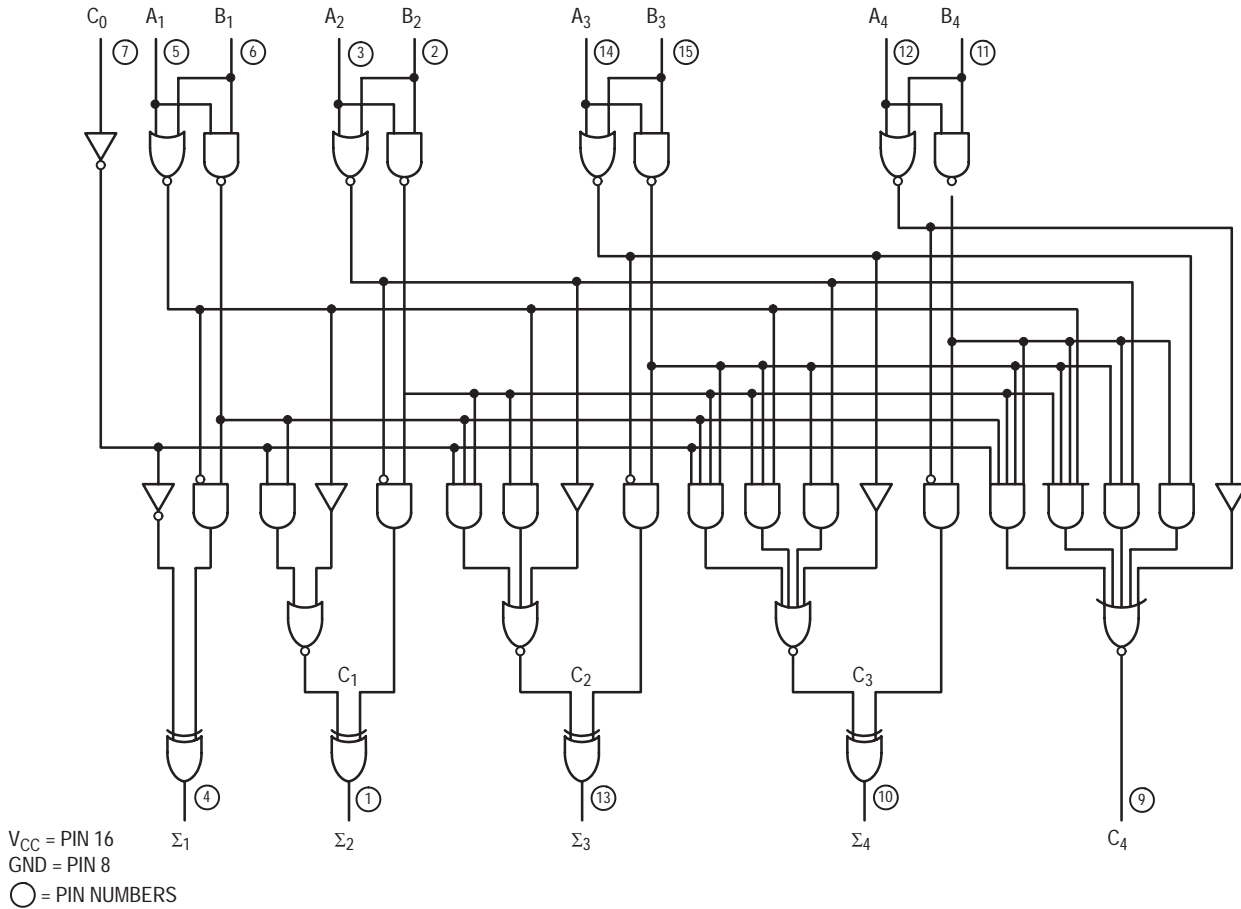
## LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS283

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ( $\Sigma_1 - \Sigma_4$ ) and outgoing carry ( $C_4$ ) outputs.

$$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

### Example:

	$C_0$	$A_1$	$A_2$	$A_3$	$A_4$	$B_1$	$B_2$	$B_3$	$B_4$	$\Sigma_1$	$\Sigma_2$	$\Sigma_3$	$\Sigma_4$	$C_4$	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus  $C_0$ ,  $A_1$ ,  $B_1$ , can be arbitrarily assigned to pins 7, 5 or 3.

# SN74LS283

## FUNCTIONAL TRUTH TABLE

C (n-1)	A <sub>n</sub>	B <sub>n</sub>	Σ <sub>n</sub>	C <sub>n</sub>
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C<sub>1</sub> – C<sub>3</sub> are generated internally  
 C<sub>0</sub> is an external input  
 C<sub>4</sub> is an output generated internally

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current	C <sub>0</sub>		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		Any A or B		40	μA	
	Input HIGH Current	C <sub>0</sub>		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
		Any A or B		0.2	mA	
I <sub>IL</sub>	Input LOW Current	C <sub>0</sub>		-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
		Any A or B		-0.8	mA	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			34	mA	V <sub>CC</sub> = MAX
	Power Supply Current Total, Output LOW			39		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS283

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $C_0$ Input to Any $\Sigma$ Output		16 15	24 24	ns	$C_L = 15\text{ pF}$ Figures 1 & 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Any A or B Input to $\Sigma$ Outputs		15 15	24 24	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $C_0$ Input to $C_4$ Output		11 11	17 22	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Any A or B Input to $C_4$ Output		11 12	17 17	ns	

## AC WAVEFORMS

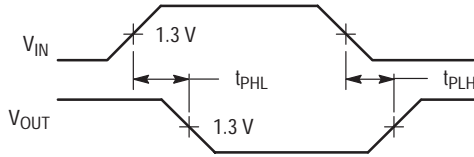


Figure 1.

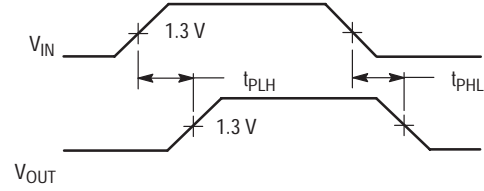


Figure 2.

# SN74LS298

## Quad 2-Input Multiplexer with Storage

The SN74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High Speed Termination Effects

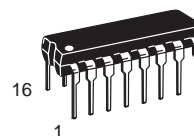
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

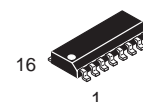


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



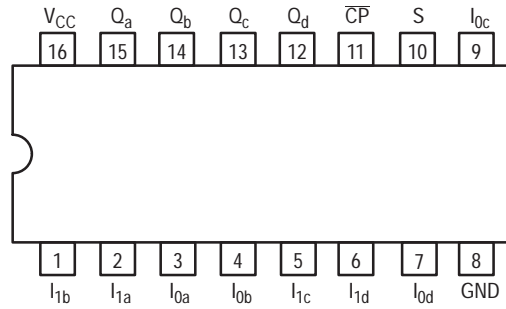
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS298N	16 Pin DIP	2000 Units/Box
SN74LS298D	16 Pin	2500/Tape & Reel

# SN74LS298

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

S	Common Select Input
$\overline{CP}$	Clock (Active LOW Going Edge) Input
$I_{0a} - I_{0d}$	Data Inputs from Source 0
$I_{1a} - I_{1d}$	Data Inputs from Source 1
$Q_a - Q_d$	Register Outputs

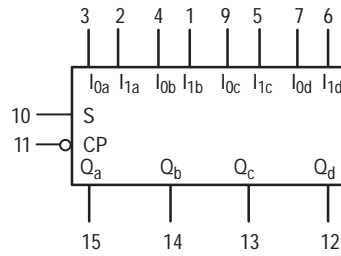
### LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
$\overline{CP}$	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	0.5 U.L.	0.25 U.L.
$Q_a - Q_d$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

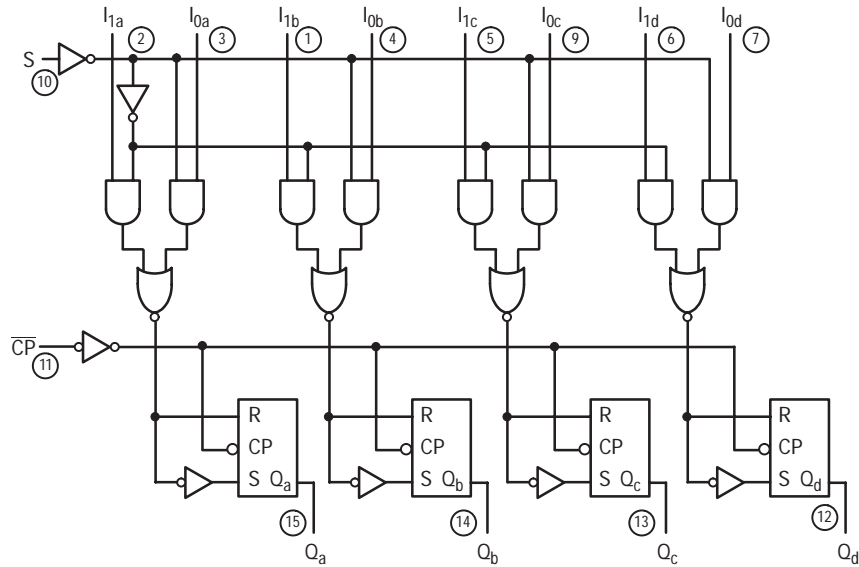
### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS298

## LOGIC OR BLOCK DIAGRAM



$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

### FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input (CP). The 4-bit

output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

### TRUTH TABLE

INPUTS			OUTPUT
S	I <sub>0</sub>	I <sub>1</sub>	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

# SN74LS298

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			21	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		18 21	27 32	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF
					ns	

## AC SET-UP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time	15			ns	
t <sub>s</sub>	Select Setup Time	25			ns	
t <sub>h</sub>	Data Hold Time	5.0			ns	
t <sub>h</sub>	Select Hold Time	0				

## DEFINITIONS OF TERMS

SETUP TIME (t<sub>s</sub>) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t<sub>h</sub>) — is defined as the minimum time following the clock transition from LOW to HIGH that the

logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.



# SN74LS298

## AC WAVEFORMS

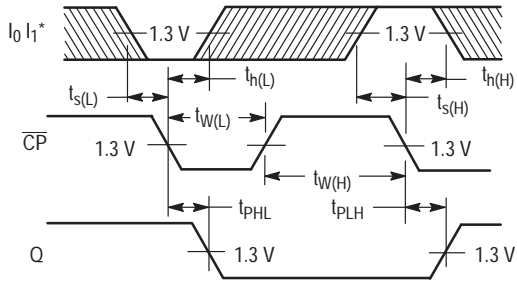


Figure 1.

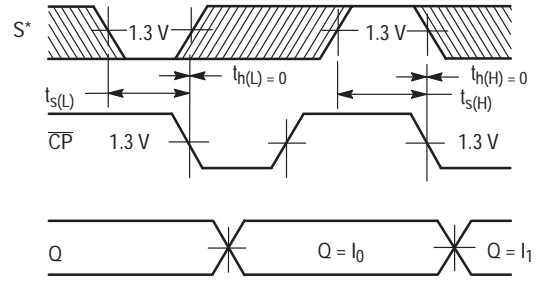


Figure 2.

\*The shaded areas indicate when the input is permitted to change for predictable output performance.

# SN74LS299

## 8-Bit Shift/Storage Register with 3-State Outputs

The SN74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops  $Q_0$  and  $Q_7$  to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High $Q_0, Q_7$			-0.4	mA
$I_{OL}$	Output Current – Low $Q_0, Q_7$			8.0	mA
$I_{OH}$	Output Current – High $I/O_0 - I/O_7$			-2.6	mA
$I_{OL}$	Output Current – Low $I/O_0 - I/O_7$			24	mA

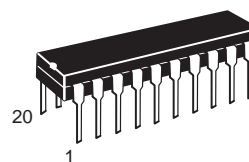


**ON Semiconductor**

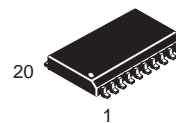
Formerly a Division of Motorola

<http://onsemi.com>

**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 738



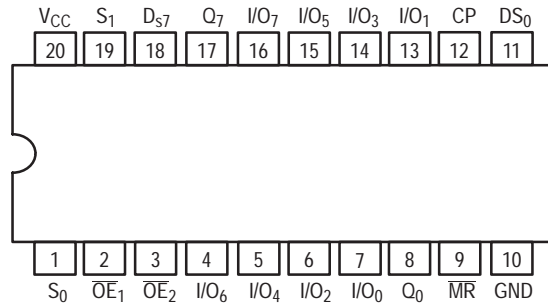
SOIC  
DW SUFFIX  
CASE 751D

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS299N	16 Pin DIP	1440 Units/Box
SN74LS299DW	16 Pin	2500/Tape & Reel

# SN74LS299

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CP	Clock Pulse (Active Positive-Going Edge) Input
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
I/O <sub>n</sub>	Parallel Data Input or Parallel Output (3-State)
OE <sub>1</sub> , OE <sub>2</sub>	3-State Output Enable (Active LOW) Inputs
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs
MR	Asynchronous Master Reset (Active LOW) Input
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs

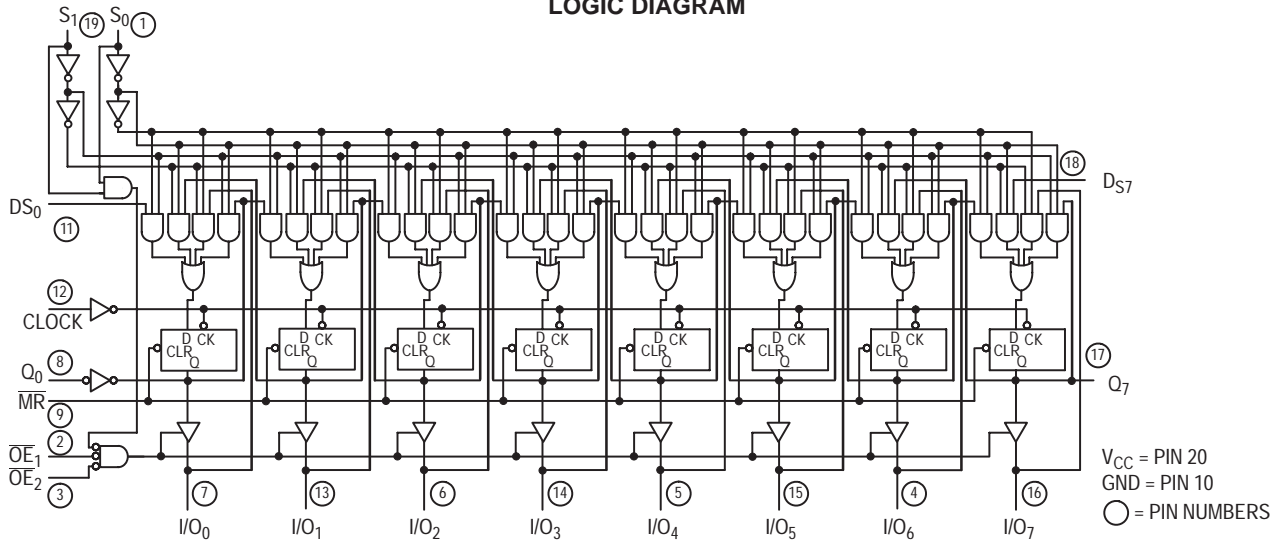
### LOADING (Note a)

	HIGH	LOW
CP	0.5 U.L.	0.25 U.L.
DS0	0.5 U.L.	0.25 U.L.
DS7	0.5 U.L.	0.25 U.L.
I/O <sub>n</sub>	0.5 U.L.	0.25 U.L.
Parallel Output (3-State)	65 U.L.	15 U.L.
OE <sub>1</sub> , OE <sub>2</sub>	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> , Q <sub>7</sub>	10 U.L.	5 U.L.
MR	0.5 U.L.	0.25 U.L.
S <sub>0</sub> , S <sub>1</sub>	1 U.L.	0.5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

## LOGIC DIAGRAM



# SN74LS299

## FUNCTION TABLE

INPUTS								RESPONSE
MR	S <sub>1</sub>	S <sub>0</sub>	OE <sub>1</sub>	OE <sub>2</sub>	CP	DS <sub>0</sub>	DS <sub>7</sub>	
L	X	X	H	X	X	X	X	Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
H	L	H	X	X	┌	D	X	Shift Right; D→Q <sub>0</sub> ; Q <sub>0</sub> →Q <sub>1</sub> ; etc. Shift Right; D→Q <sub>0</sub> & I/O <sub>0</sub> ; Q <sub>0</sub> →Q <sub>1</sub> & I/O <sub>1</sub> ; etc.
H	L	H	L	L	└	D	X	
H	H	L	X	X	┌	X	D	Shift Left; D→Q <sub>7</sub> ; Q <sub>7</sub> →Q <sub>6</sub> ; etc. Shift Left; D→Q <sub>7</sub> & I/O <sub>7</sub> ; Q <sub>7</sub> →Q <sub>6</sub> & I/O <sub>6</sub> ; etc.
H	H	L	L	L	└	X	D	
H	H	H	X	X	┌	X	X	Parallel Load; I/O <sub>n</sub> →Q <sub>n</sub>
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O <sub>n</sub> = Q <sub>n</sub>

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

# SN74LS299

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage I/O <sub>0</sub> -I/O <sub>7</sub>	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	
V <sub>OH</sub>	Output HIGH Voltage Q <sub>0</sub> , Q <sub>7</sub>	2.7	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	
V <sub>OL</sub>	Output LOW Voltage I/O <sub>0</sub> -I/O <sub>7</sub>		0.25	0.4	V	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	I <sub>OL</sub> = 24 mA	
V <sub>OL</sub>	Output LOW Voltage I/O <sub>0</sub> -I/O <sub>7</sub>			0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
				0.5	V	I <sub>OL</sub> = 8.0 mA	
I <sub>OZH</sub>	Output Off Current HIGH I/O <sub>0</sub> -I/O <sub>7</sub>			40	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW I/O <sub>0</sub> -I/O <sub>7</sub>			-400	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current	Others		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
		S <sub>0</sub> , S <sub>1</sub> , I/O <sub>0</sub> -I/O <sub>7</sub>		40	μA		
		Others		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
		S <sub>0</sub> , S <sub>1</sub>		0.2	mA		
		I/O <sub>0</sub> -I/O <sub>7</sub>		0.1	mA		
I <sub>IL</sub>	Input LOW Current	Others		-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
		S <sub>0</sub> , S <sub>1</sub>		-0.8	mA		
I <sub>OS</sub>	Short Circuit Current (Note 1)	Q <sub>0</sub> , Q <sub>7</sub>	-20	-100	mA	V <sub>CC</sub> = MAX	
		I/O <sub>0</sub> -I/O <sub>7</sub>	-30	-130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			53	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS299

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Clock Frequency	25	35		MHz	$C_L = 15\text{ pF}$
$t_{PHL}$ $t_{PLH}$	Propagation Delay, Clock to $Q_0$ or $Q_7$		26 22	39 33	ns	
$t_{PHL}$	Propagation Delay, Clear to $Q_0$ or $Q_7$		27	40	ns	
$t_{PHL}$ $t_{PLH}$	Propagation Delay, Clock to $I/O_0$ – $I/O_7$		26 17	39 25	ns	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$
$t_{PHL}$	Propagation Delay, Clear to $I/O_0$ – $I/O_7$		26	40	ns	
$t_{PZH}$ $t_{PZL}$	Output Enable Time		13 19	21 30	ns	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time		10 10	15 15	ns	$C_L = 5.0\text{ pF}$

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock Pulse Width HIGH	25			ns	$V_{CC} = 5.0\text{ V}$
$t_W$	Clock Pulse Width LOW	13			ns	
$t_W$	Clear Pulse Width LOW	20			ns	
$t_s$	Data Setup Time	20			ns	
$t_s$	Select Setup Time	35			ns	
$t_h$	Data Hold Time	0			ns	
$t_h$	Select Hold Time	10			ns	
$t_{rec}$	Recovery Time	20			ns	

# SN74LS299

## 3-STATE WAVEFORMS

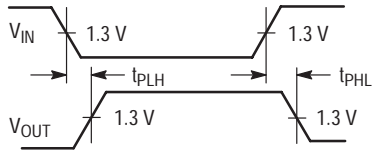


Figure 1.

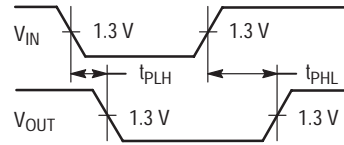


Figure 2.

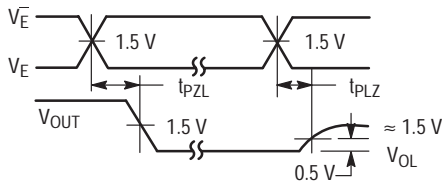


Figure 3.

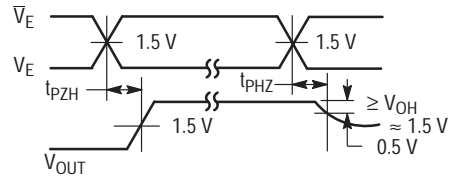
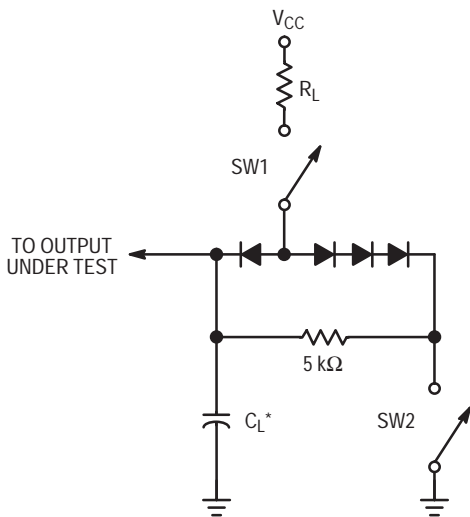


Figure 4.

## AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

Figure 5.

## SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

# SN74LS365A SN74LS367A SN74LS368A



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## 3-State Hex Buffers

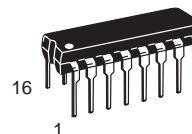
These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

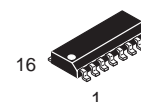
**LOW  
POWER  
SCHOTTKY**

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-2.6	mA
$I_{OL}$	Output Current – Low			24	mA



**PLASTIC  
N SUFFIX  
CASE 648**



**SOIC  
D SUFFIX  
CASE 751B**

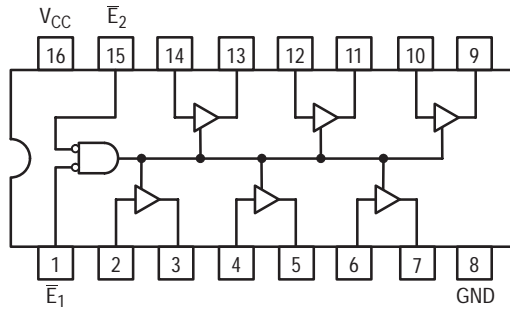
### ORDERING INFORMATION

Device	Package	Shipping
SN74LS365AN	16 Pin DIP	2000 Units/Box
SN74LS365AD	16 Pin	2500/Tape & Reel
SN74LS367AN	16 Pin DIP	2000 Units/Box
SN74LS367AD	16 Pin	2500/Tape & Reel
SN74LS368AN	16 Pin DIP	2000 Units/Box
SN74LS368AD	16 Pin	2500/Tape & Reel



SN74LS365A SN74LS367A SN74LS368A

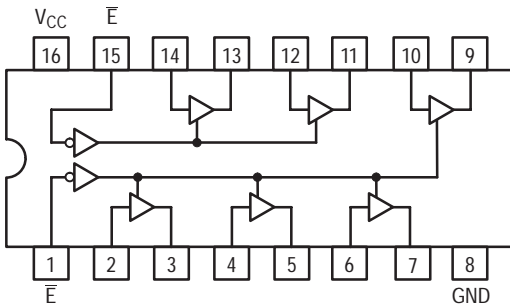
SN74LS365A  
HEX 3-STATE BUFFER WITH  
COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

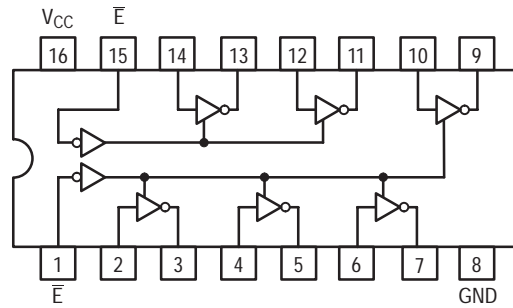
SN74LS367A  
HEX 3-STATE BUFFER  
SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
E	D	
L	L	L
L	H	H
H	X	(Z)

SN74LS368A  
HEX 3-STATE INVERTER BUFFER  
SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
E	D	
L	L	H
L	H	L
H	X	(Z)

# SN74LS365A SN74LS367A SN74LS368A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current E Inputs			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
	D Inputs			-20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.5 V Either $\bar{E}$ Input at 2.0 V
				-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V Both $\bar{E}$ Inputs at 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current LS365A, 367A			24	mA	V <sub>CC</sub> = MAX
	LS368A			21		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS365A/LS367A			LS366A/LS368A				
		Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay		10 9.0	16 22		7.0 12	15 18	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		19 24	35 40		18 28	35 45	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time			30 35			32 35	ns	C <sub>L</sub> = 5.0 pF

# SN74LS373 SN74LS374

## Octal Transparent Latch with 3-State Outputs; Octal D-Type Flip-Flop with 3-State Output

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

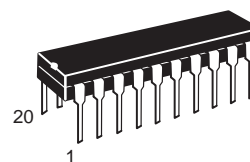
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-2.6	mA
$I_{OL}$	Output Current – Low			24	mA

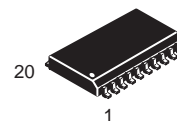


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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 738**



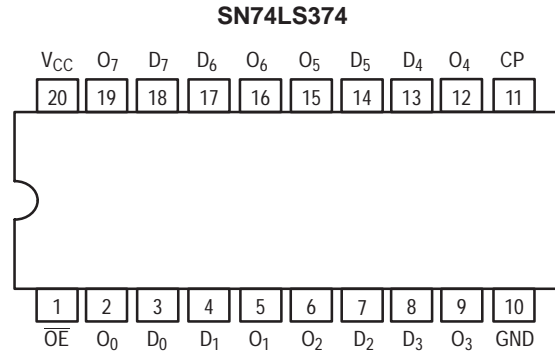
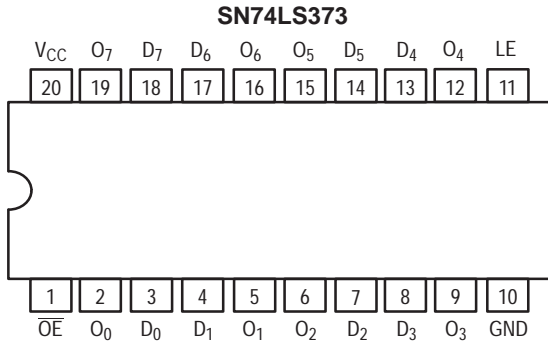
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS373N	16 Pin DIP	1440 Units/Box
SN74LS373DW	16 Pin	2500/Tape & Reel
SN74LS374N	16 Pin DIP	1440 Units/Box
SN74LS374DW	16 Pin	2500/Tape & Reel

# SN74LS373 SN74LS374

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
 The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

D<sub>0</sub> – D<sub>7</sub> Data Inputs  
 LE Latch Enable (Active HIGH) Input  
 CP Clock (Active HIGH Going Edge) Input  
 $\overline{O\!E}$  Output Enable (Active LOW) Input  
 O<sub>0</sub> – O<sub>7</sub> Outputs

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.



### TRUTH TABLE

#### LS373

D <sub>n</sub>	LE	$\overline{O\!E}$	O <sub>n</sub>
H	H	L	H
L	H	L	L
X	L	L	Q <sub>0</sub>
X	X	H	Z*

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

#### LS374

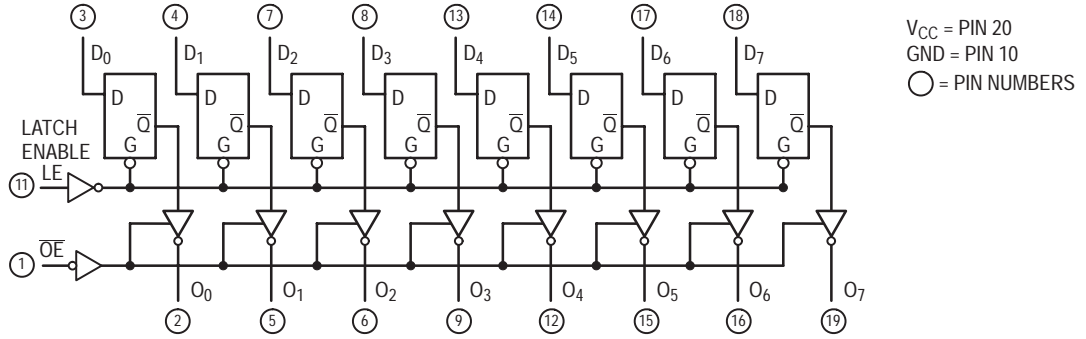
D <sub>n</sub>	LE	$\overline{O\!E}$	O <sub>n</sub>
H		L	H
L		L	L
X	X	H	Z*

\* Note: Contents of flip-flops unaffected by the state of the Output Enable input ( $\overline{O\!E}$ ).

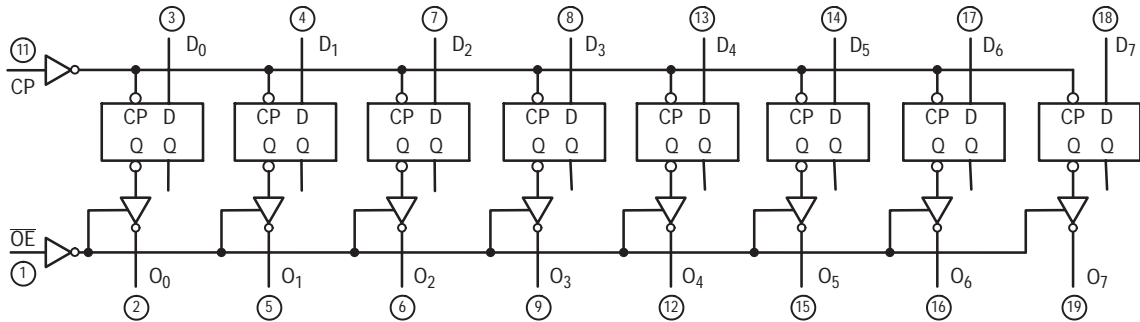
# SN74LS373 SN74LS374

## LOGIC DIAGRAMS

### SN74LS373



### SN74LS374



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.4	3.1		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{OZH}$	Output Off Current HIGH			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{OUT} = 2.7 \text{ V}$
$I_{OZL}$	Output Off Current LOW			-20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{OUT} = 0.4 \text{ V}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			40	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## SN74LS373 SN74LS374

### AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
$f_{\text{MAX}}$	Maximum Clock Frequency				35	50		MHz	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay, Data to Output		12 12	18 18				ns	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time		15 25	28 36		20 21	28 28	ns	
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time		12 15	20 25		12 15	20 25	ns	$C_L = 5.0\text{ pF}$

### AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
$t_W$	Clock Pulse Width	15		15		ns
$t_s$	Setup Time	5.0		20		ns
$t_h$	Hold Time	20		0		ns

### DEFINITION OF TERMS

**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

# SN74LS373 SN74LS374

## SN74LS373

### AC WAVEFORMS

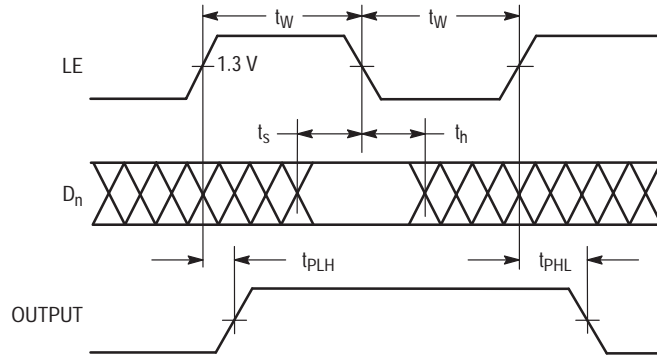


Figure 1.

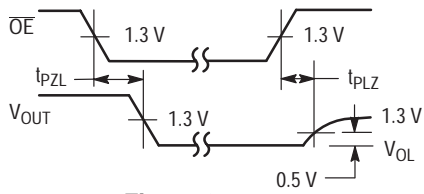


Figure 2.

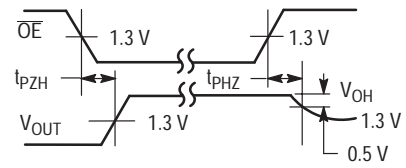
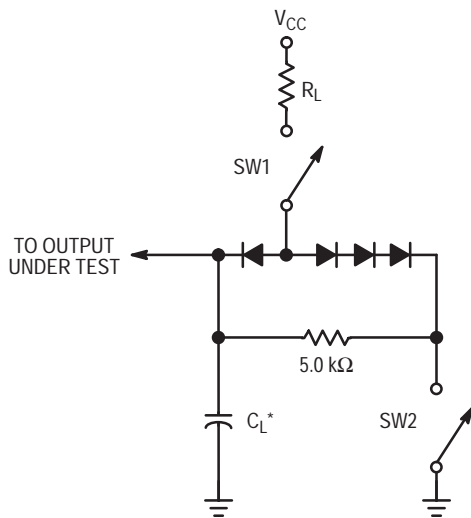


Figure 3.

### AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

Figure 4.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

# SN74LS373 SN74LS374

## SN74LS374

### AC WAVEFORMS

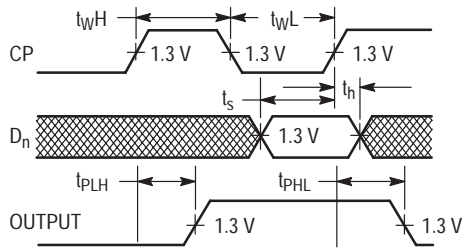


Figure 5.

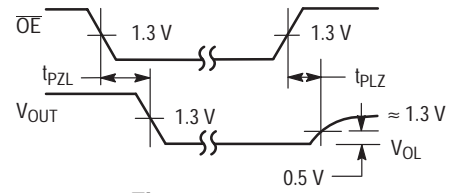


Figure 6.

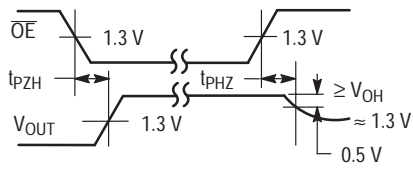
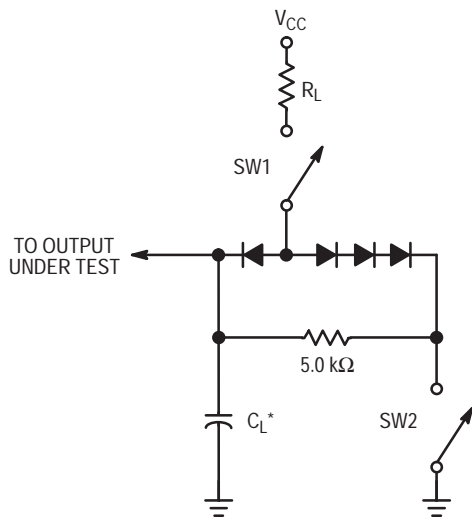


Figure 7.

### AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

Figure 8.



# SN74LS377

## Octal D Flip-Flop with Enable

The SN74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

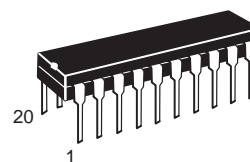
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

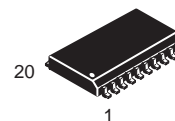


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**PLASTIC  
N SUFFIX  
CASE 738**



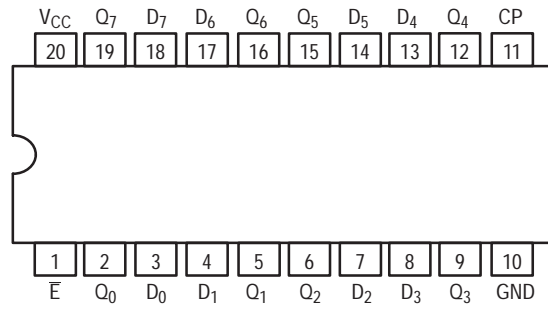
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS377N	16 Pin DIP	1440 Units/Box
SN74LS377DW	16 Pin	2500/Tape & Reel

# SN74LS377

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version  
has the same pinouts  
(Connection Diagram) as  
the Dual In-Line Package.

### PIN NAMES

$\bar{E}$	Enable (Active LOW) Input
$D_0 - D_3$	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$Q_0 - Q_3$	True Outputs
$\bar{Q}_0 - \bar{Q}_3$	Complemented Outputs

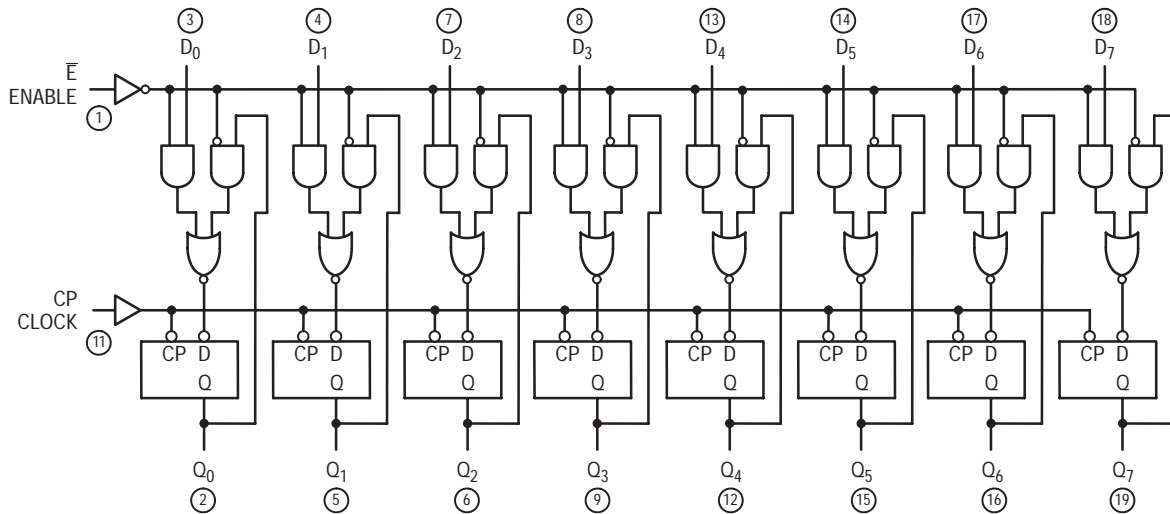
### LOADING (Note a)

	HIGH	LOW
$\bar{E}$	0.5 U.L.	0.25 U.L.
$D_0 - D_3$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
$\bar{Q}_0 - \bar{Q}_3$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC DIAGRAM



# SN74LS377

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			28	mA	V <sub>CC</sub> = MAX, NOTE 1

NOTE: With all inputs open and GND applied to all data and enable inputs, I<sub>CC</sub> is measured after a momentary GND, then 4.5 V is applied to clock.  
 Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	40		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		17 18	27 27	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t <sub>W</sub>	Any Pulse Width		20			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Data Setup Time		20			ns	
t <sub>s</sub>	Enable Setup Time	Inactive — State	10			ns	
		Active — State	25			ns	
t <sub>h</sub>	Any Hold Time		5.0			ns	

## DEFINITION OF TERMS




**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the

logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

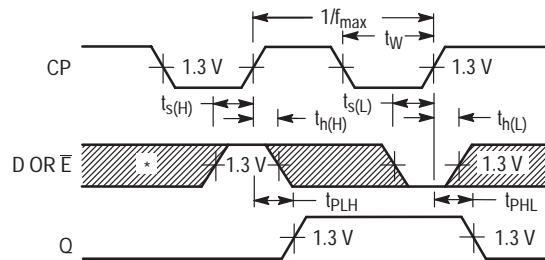
# SN74LS377

## TRUTH TABLE

$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
H		X	No Change	No Change
L		H	H	L
L		L	L	H

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial

## AC WAVEFORM



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

# SN74LS393

## Dual 4-Stage Binary Counter

The SN74LS393 contains a pair of high-speed 4-stage ripple counters.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

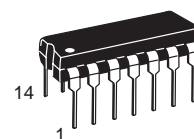


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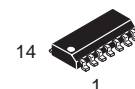
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N SUFFIX  
CASE 646**



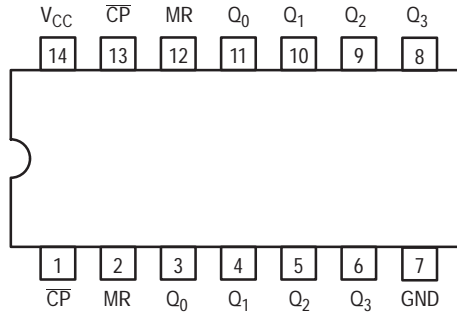
**SOIC  
D SUFFIX  
CASE 751A**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS393N	14 Pin DIP	2000 Units/Box
SN74LS393D	14 Pin	2500/Tape & Reel

# SN74LS393

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version  
has the same pinouts  
(Connection Diagram) as  
the Dual In-Line Package.

### PIN NAMES

$\overline{CP}$	Clock (Active LOW Going Edge) Input to +16 (LS393)
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to +2 (LS390)
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to +5 (LS390)
MR	Master Reset (Active HIGH) Input
$Q_0 - Q_3$	Flip-Flop Outputs

### LOADING (Note a)

	HIGH	LOW
$\overline{CP}$	0.5 U.L.	1.0 U.L.
$\overline{CP}_0$	0.5 U.L.	1.0 U.L.
$\overline{CP}_1$	0.5 U.L.	1.5 U.L.
MR	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

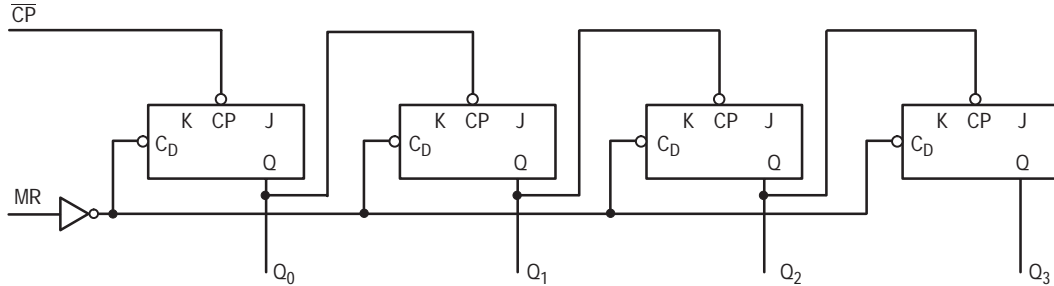
# SN74LS393

## FUNCTIONAL DESCRIPTION

Each half of the SN74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do

not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

SN74LS393 LOGIC DIAGRAM (one half shown)



TRUTH TABLE

COUNT	OUTPUTS			
	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level

# SN74LS393

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current	MR		-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
		$\overline{CP}$ , $\overline{CP}_0$		-1.6	mA	
		$\overline{CP}_1$		-2.4	mA	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			26	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency $\overline{CP}_0$ to Q <sub>0</sub>	25	35		MHz	C <sub>L</sub> = 15 pF
f <sub>MAX</sub>	Maximum Clock Frequency $\overline{CP}_1$ to Q <sub>1</sub>	20			MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\overline{CP}$ to Q <sub>0</sub>		12 13	20 20	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	$\overline{CP}$ to Q <sub>3</sub>		40 40	60 60	ns	
t <sub>PHL</sub>	MR to Any Output		24	39	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	MR Pulse Width	20			ns	
t <sub>rec</sub>	Recovery Time	25			ns	



# SN74LS393

## AC WAVEFORMS

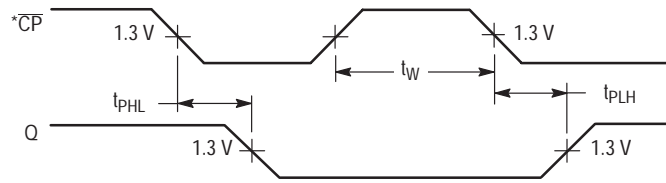


Figure 1.

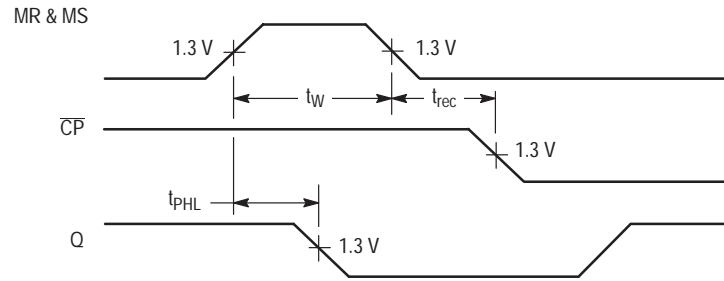


Figure 2.

\*The number of Clock Pulses required between  $t_{PHL}$  and  $t_{PLH}$  measurements can be determined from the appropriate Truth Table.

# SN74LS541

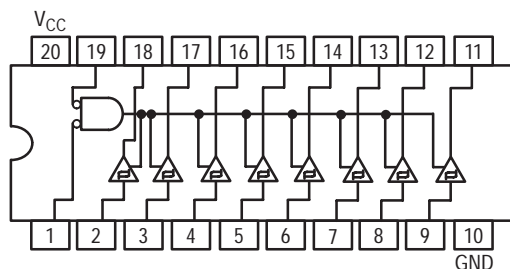
## Octal Buffer/Line Driver with 3-State Outputs

The SN74LS541 is an octal buffer and line driver with the same functions as the LS241, but with pinouts on the opposite side of the package.

This device type is designed to be used as a memory address driver, clock driver and bus-oriented transmitter/receiver. This device is especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

- Hysteresis at Inputs to Improve Noise Margin
- PNP Inputs Reduce Loading
- 3-State Outputs Drive Bus Lines
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Input Clamp Diodes Limit High-Speed Termination Effects

### LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)



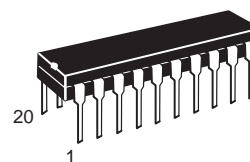
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-15	mA
$I_{OL}$	Output Current – Low			24	mA

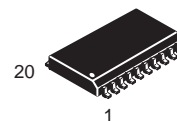


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**PLASTIC  
N SUFFIX  
CASE 738**



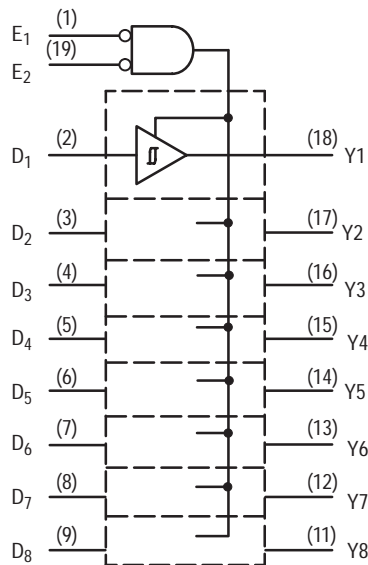
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS541N	16 Pin DIP	1440 Units/Box
SN74LS541DW	16 Pin	2500/Tape & Reel

# SN74LS541

## BLOCK DIAGRAM



INPUTS			OUTPUTS	
E <sub>1</sub>	E <sub>2</sub>	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -3.0 mA
		2.0			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IL</sub> = 0.5 V
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	0.2	0.4		V	V <sub>CC</sub> = MIN
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			32	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			52	mA	
	Total Output 3-State			55	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS541

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub>	Propagation Delay, Data to Output		12	15	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PHL</sub>			12	18		
t <sub>PZH</sub>	Output Enable Time to HIGH Level		15	32	ns	
t <sub>PZL</sub>	Output Enable Time to LOW Level		20	38	ns	
t <sub>PHZ</sub>	Output Disable Time to HIGH Level		10	18	ns	C <sub>L</sub> = 5.0 pF
t <sub>PLZ</sub>	Output Disable Time to LOW Level		15	29	ns	

## AC WAVEFORMS

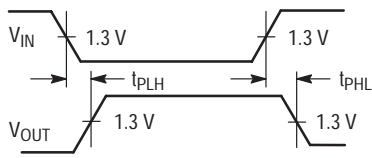


Figure 1.

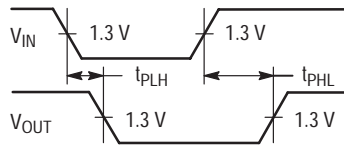


Figure 2.

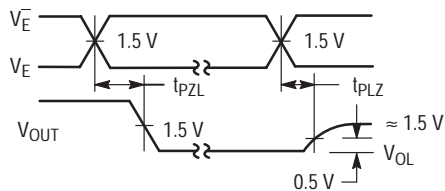


Figure 3.

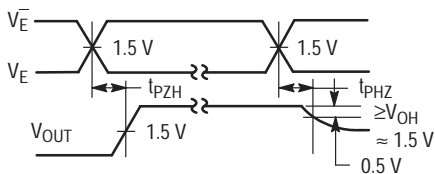
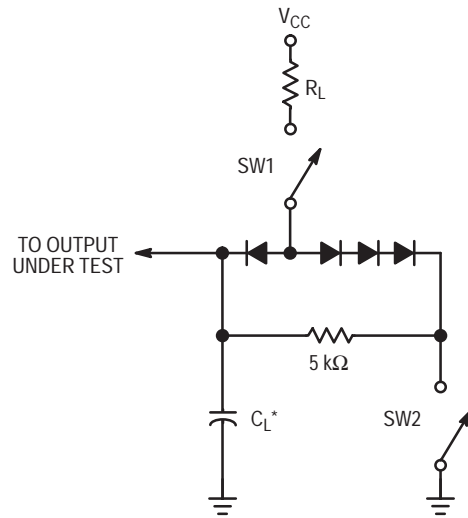


Figure 4.



### SWITCH POSITIONS

SYMBOL	SW1	SW2
t <sub>PZH</sub>	Open	Closed
t <sub>PZL</sub>	Closed	Open
t <sub>PLZ</sub>	Closed	Closed
t <sub>PHZ</sub>	Closed	Closed

Figure 5.

# SN74LS640 SN74LS641 SN74LS642 SN74LS645

## Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ( $\bar{G}$ ) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\bar{G}$	DIR	LS640 LS642	LS641 LS645
		L	L
L	H	$\bar{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

### GUARANTEED OPERATING RANGES (SN74LS640, SN74LS645)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-3.0	mA
				-15	mA
$I_{OL}$	Output Current – Low			24	mA

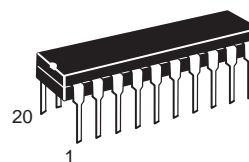
### GUARANTEED OPERATING RANGES (SN74LS641, SN74LS642)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$V_{OH}$	Output Voltage – High			5.5	V
$I_{OL}$	Output Current – Low			24	mA

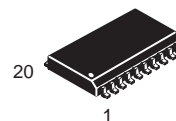


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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 738



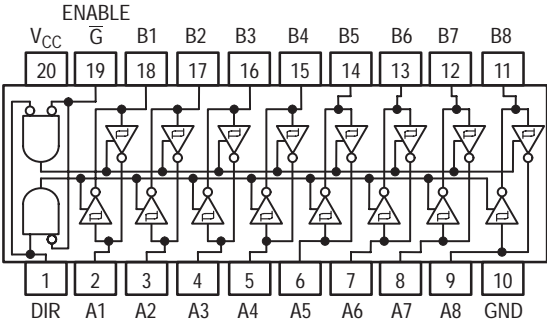
SOIC  
DW SUFFIX  
CASE 751D

### ORDERING INFORMATION

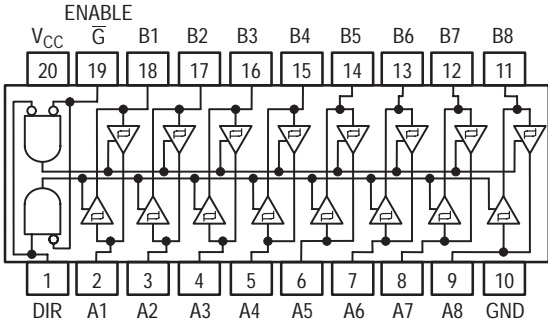
Device	Package	Shipping
SN74LS640N	16 Pin DIP	1440 Units/Box
SN74LS640DW	16 Pin	2500/Tape & Reel
SN74LS641N	16 Pin DIP	1440 Units/Box
SN74LS641DW	16 Pin	2500/Tape & Reel
SN74LS642N	16 Pin DIP	1440 Units/Box
SN74LS642DW	16 Pin	2500/Tape & Reel
SN74LS645N	16 Pin DIP	1440 Units/Box
SN74LS645DW	16 Pin	2500/Tape & Reel

**SN74LS640 SN74LS641 SN74LS642 SN74LS645**

**CONNECTION DIAGRAMS DIP (TOP VIEW)**



**SN74LS640  
SN74LS642**



**SN74LS641  
SN74LS645**

# SN74LS640 SN74LS641 SN74LS642 SN74LS645

## SN74LS640 • SN74LS645

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = 3.0 mA
		2.0			V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current LOW			-400	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current	A or B, DIR or $\bar{G}$		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		DIR or $\bar{G}$		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
		A or B		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 5.5 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Output Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			70	mA	V <sub>CC</sub> = MAX
	Total Output HIGH			90		
	Total at HIGH Z			95		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

### AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS640			LS645				
		Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A to B		6.0	10		8.0	15	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
			8.0	15		11	15		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay B to A		6.0	10		8.0	15		
			8.0	15		11	15		
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\bar{G}$ , DIR to A		31	40		31	40		
			23	40		26	40		
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\bar{G}$ , DIR to B		31	40		31	40		
			23	40		26	40		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\bar{G}$ , DIR to A		15	25		15	25	ns	C <sub>L</sub> = 5.0 pF
			15	25		15	25		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time $\bar{G}$ , DIR to B		15	25		15	25		
			15	25		15	25		

**SN74LS640 SN74LS641 SN74LS642 SN74LS645**

**SN74LS641 • SN74LS642**

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
I <sub>OH</sub>	Output HIGH Current			100	μA	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				-0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			70	mA	V <sub>CC</sub> = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

**AC CHARACTERISTICS** (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\bar{G}$ , DIR to A		23 34	40 50		26 43	40 60	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\bar{G}$ , DIR to B		25 37	40 50		28 39	40 60	ns	



# SN74LS670

## 4 x 4 Register File with 3-State Outputs

The TTL/MSI SN74LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

- Simultaneous Read/Write Operation
- Expandable to 512 Words by n-Bits
- Typical Access Time to 20 ns
- 3-State Outputs for Expansion
- Typical Power Dissipation of 125 mW

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-2.6	mA
I <sub>OL</sub>	Output Current – Low			24	mA

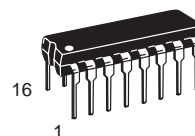


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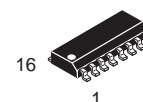
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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 648**



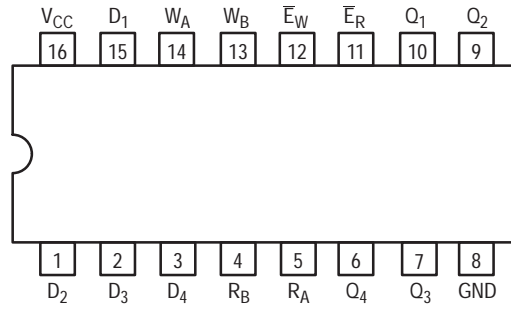
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS670N	16 Pin DIP	2000 Units/Box
SN74LS670D	16 Pin	2500/Tape & Reel

# SN74LS670

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

D <sub>1</sub> - D <sub>4</sub>	Data Inputs
W <sub>A</sub> , W <sub>B</sub>	Write Address Inputs
$\bar{E}_W$	Write Enable (Active LOW) Input
R <sub>A</sub> , R <sub>B</sub>	Read Address Inputs
$\bar{E}_R$	Read Enable (Active LOW) Input
Q <sub>1</sub> - Q <sub>4</sub>	Outputs

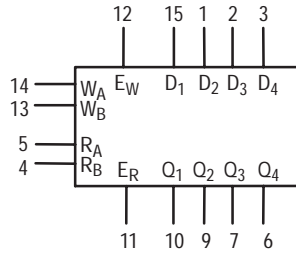
### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
1.0 U.L.	0.5 U.L.
0.5 U.L.	0.25 U.L.
1.5 U.L.	0.75 U.L.
65 U.L.	15 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL

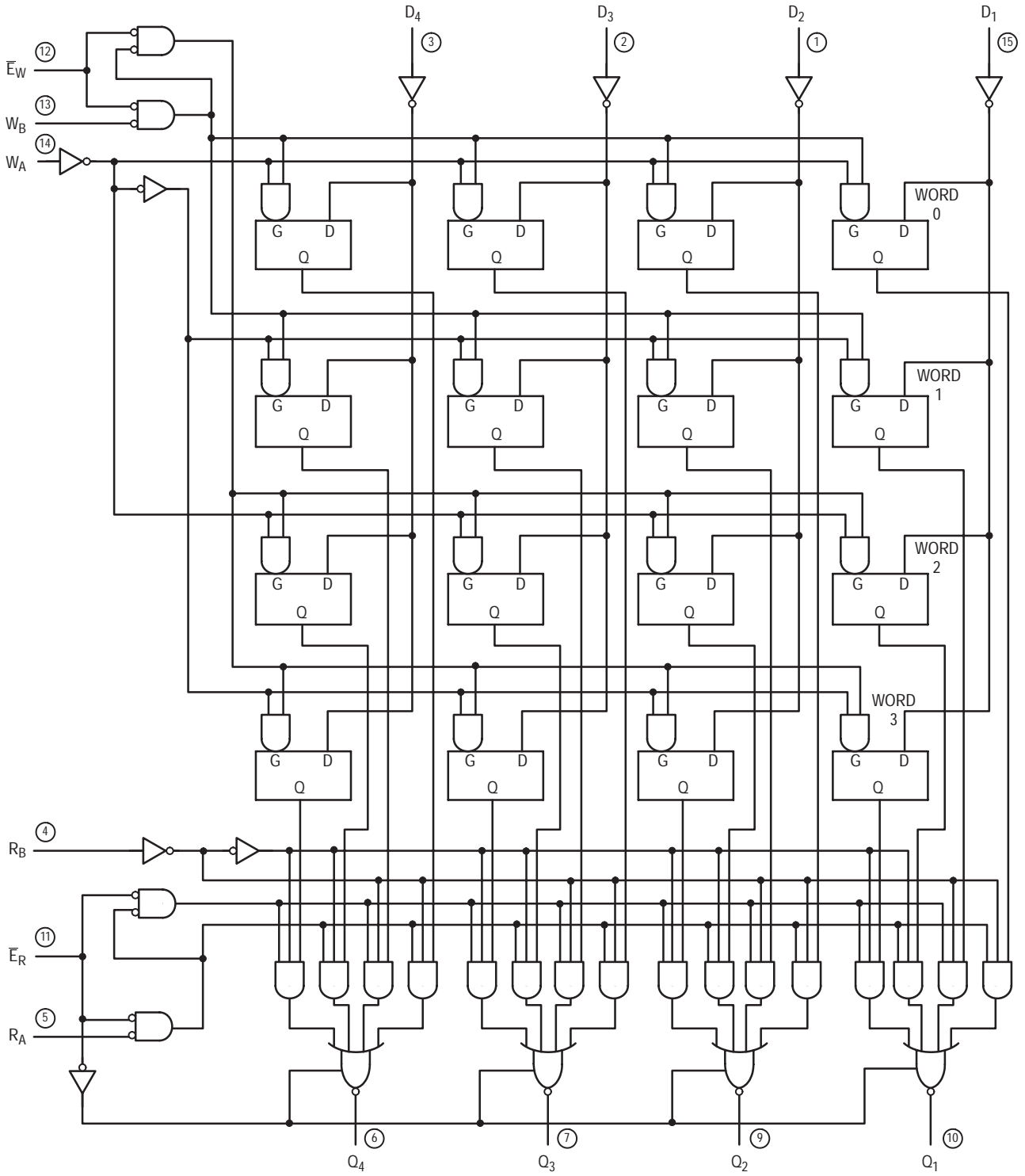


V<sub>CC</sub> = PIN 16

GND = PIN 8

# SN74LS670

## LOGIC DIAGRAM



V<sub>CC</sub> = PIN 16  
GND = PIN 8  
○ = PIN NUMBERS

# SN74LS670

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.4	3.1		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
			0.35	0.5	V	
$I_{OZH}$	Output Off Current HIGH			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_O = 2.7 \text{ V}$
$I_{OZL}$	Output Off Current LOW			-20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_O = 0.4 \text{ V}$
$I_{IH}$	Input HIGH Current D, R, W $E_W$ $E_R$			20 40 60	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
	D, R, W $E_W$ $E_R$			0.1 0.2 0.3	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current D, R, W $E_W$ $E_R$			-0.4 -0.8 -1.2	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			50	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS670

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $R_A$ or $R_B$ to Output		23 25	40 45	ns	$V_{CC} = 5.0\text{ V}$ , $C_L = 45\text{ pF}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\bar{E}_W$ to Output		26 28	45 50	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Data to Output		25 23	45 40	ns	
$t_{PZH}$ $t_{PZL}$	Output Enable Time		15 22	35 40	ns	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time		16 30	35 50	ns	$C_L = 5.0\text{ pF}$

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
$t_s$	Setup Time, (D)	10			ns	
$t_s$	Setup Time, (W)	15			ns	
$t_h$	Hold Time, (D)	15			ns	
$t_h$	Hold Time, (W)	5.0			ns	
$t_{rec}$	Recovery Time	25			ns	

## AC WAVEFORMS

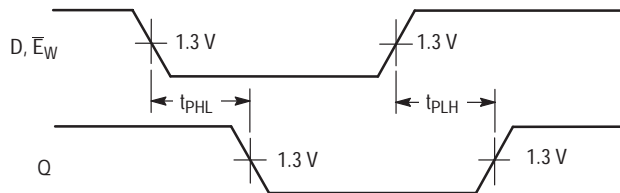


Figure 1.

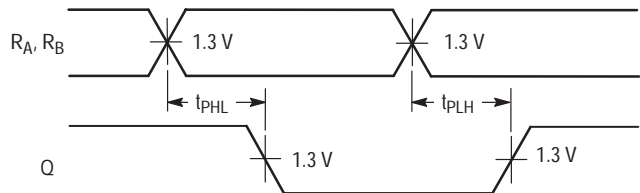


Figure 2.

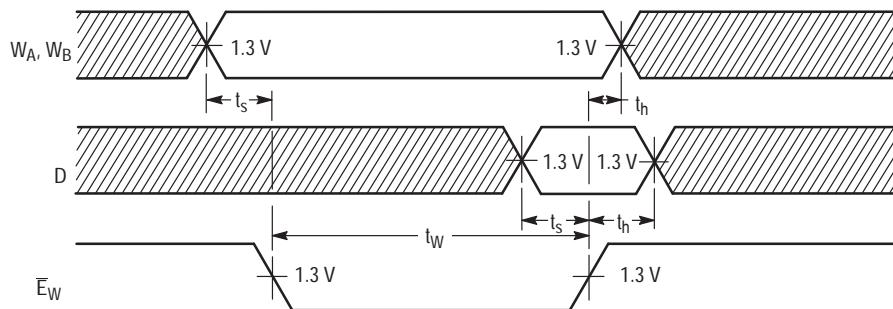


Figure 3.

# SN74LS682 SN74LS684 SN74LS688

## 8-Bit Magnitude Comparators

The SN74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide  $\overline{P=Q}$  outputs and the LS682 and LS684 have  $\overline{P>Q}$  outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 k $\Omega$  pullup resistor on the Q inputs for analog or switch data.

TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

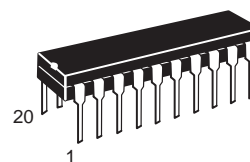
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			– 0.4	mA
I <sub>OL</sub>	Output Current – Low			24	mA

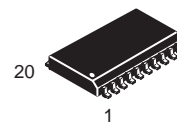


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<http://onsemi.com>

**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 738**



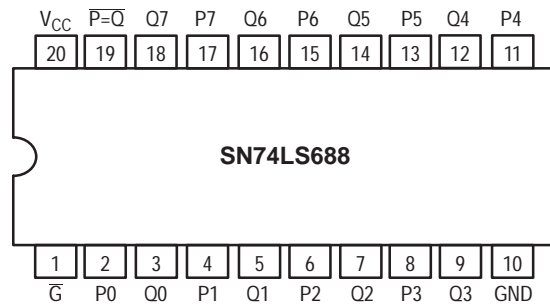
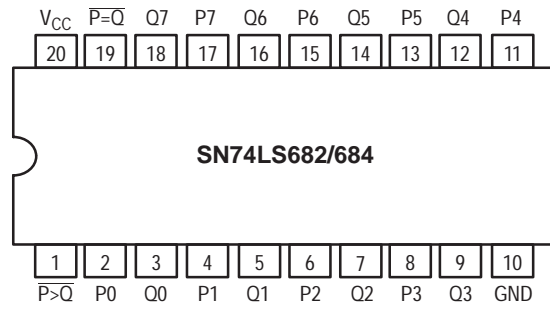
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS682N	16 Pin DIP	1440 Units/Box
SN74LS682DW	16 Pin	2500/Tape & Reel
SN74LS684N	16 Pin DIP	1440 Units/Box
SN74LS684DW	16 Pin	2500/Tape & Reel
SN74LS688N	16 Pin DIP	1440 Units/Box
SN74LS688DW	16 Pin	2500/Tape & Reel

# SN74LS682 SN74LS684 SN74LS688

## CONNECTION DIAGRAMS (TOP VIEW)



## FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}, \overline{GT}$	G2		
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = HIGH Level, L = LOW Level, X = Irrelevant

# SN74LS682 SN74LS684 SN74LS688

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

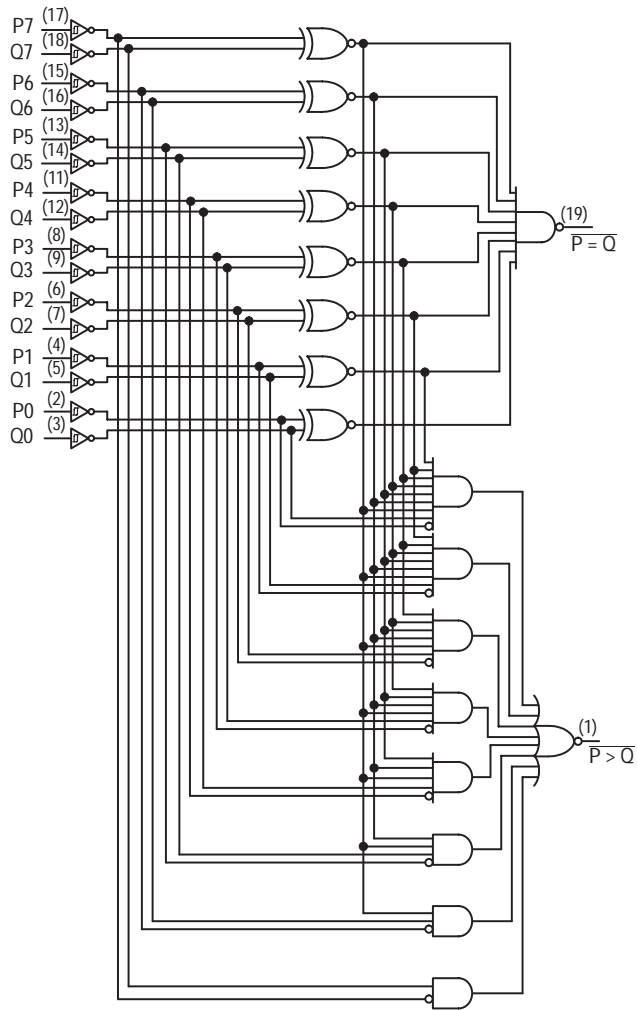
Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$	
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$	
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$	
		LS682-Q Inputs			0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 5.5 \text{ V}$
		Others			0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current	LS682-Q Inputs			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
		Others			-0.2	mA	
$I_{OS}$	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$	
$I_{CC}$	Power Supply Current	LS682			70	mA	$V_{CC} = \text{MAX}$
		LS684			65	mA	
		LS688			65	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

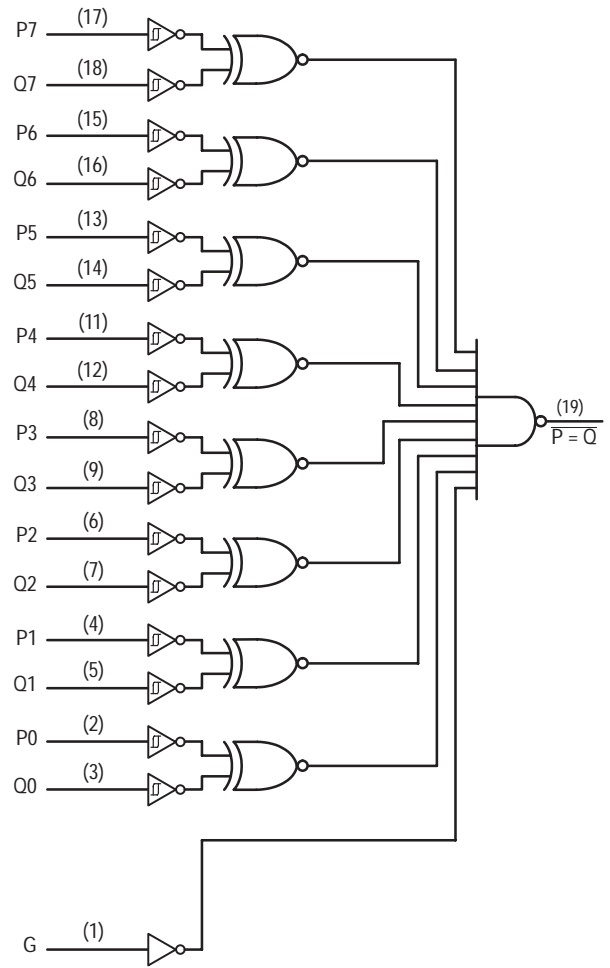


# SN74LS682 SN74LS684 SN74LS688

## LOGIC DIAGRAMS



SN74LS682 and LS684



SN74LS688

# SN74LS682 SN74LS684 SN74LS688

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

### SN74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

### SN74LS684

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

### SN74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, $\overline{G}$ , $\overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	



# CHAPTER 5

## Reliability Data

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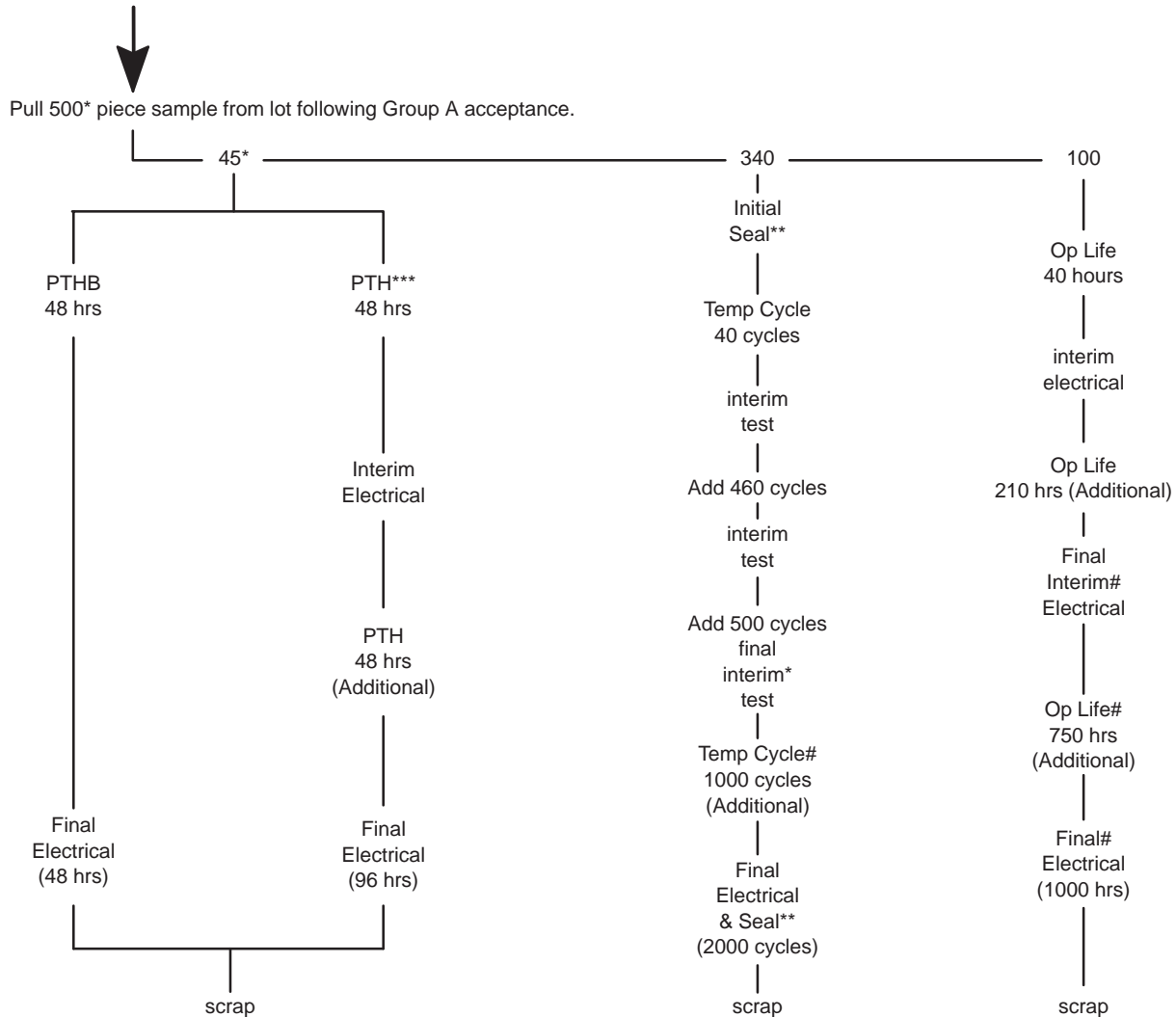
# **“RAP” Reliability Audit Program for Logic Integrated Circuits**

## **1.0 INTRODUCTION**

The Reliability Audit Program developed in March 1977 is the ON Semiconductor internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are available at all sales offices.

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.

## 2.0 RAP TEST FLOW



# One sample per month for LS, 10H, 10K, MG CMOS, and HSL CMOS.

\* PTHB or PTH not required for hermetic products; reduce total sample size to 450 pcs.  
Additional sample reductions for high pin-count devices per TABLE II notes.

\*\* Seal (Fine & Gross Leak) required for hermetic products.

\*\*\* PTH to be used when sockets for PTHB are not available.

### 3.0 TEST CONDITIONS AND COMMENTS

**PTHB** — 15 psig/121°C/100% RH at rated  $V_{CC}$  or  $V_{EE}$  — to be performed on plastic encapsulated devices only.

**TEMP CYCLING** — MIL-STD-883, Method 1010, Condition C, -65°C/+150°C.

**OP LIFE** — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias),  $T_A = 145^\circ\text{C}$ .

### NOTES:

1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each logic I/C product family (MECL, TTL, etc.) and will include all assembly locations.
5. 16 hrs. PTHB is equivalent to approximately 800 hours of 85°C/85% RH THB for  $V_{CC} \leq 15\text{ V}$ .
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

# CHAPTER 6

## Package Information Including Surface Mount

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## BIPOLAR LOGIC SURFACE MOUNT

### WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and/or offer increased functions with the same size product.

### SURFACE MOUNT AVAILABILITY

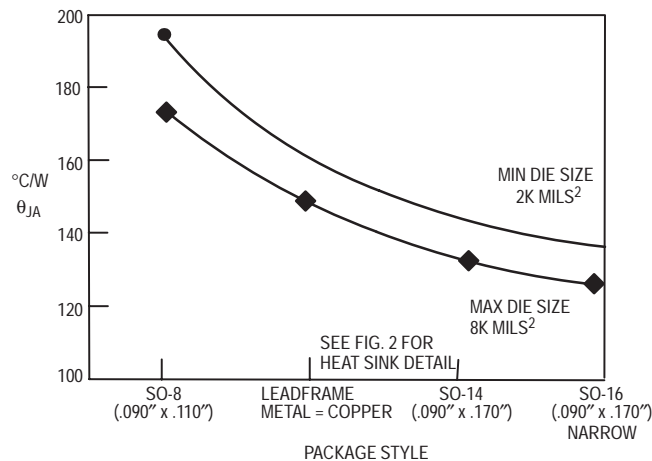
Bipolar Logic is currently offering LS-TTL in production quantities in SOIC packages.

Refer to the following Selector Guide (SG366/D) which indicate availability and package type for these families.

These families may be ordered in rails or on Tape and Reel. Refer to Tape and Reel information for ordering details.

### THERMAL DATA

The power dissipation of surface mount packages is dependent on many factors that must be taken into consideration in the initial board design. The board material, the board surface metal thickness, pad area and the proximity to other heat generating components all have a bearing on the device dissipation capability.



DATA TAKEN USING PHILIPS SO TEST BOARD # 7322-078, 80873

Figure 1. Thermal Resistance, Junction-To-Ambient (°C/W)

Measurement specimens are solder mounted on printed circuit card 19 mm × 28 mm × 1.5 mm in still air. No auxiliary thermal condition aids are used.

This data was collected using thermal test die in 20-pin PLCC packages on PLCC test boards (2.24" x 2.24" x .062" glass epoxy, type FR-4, with solder coated 1 oz./sq. ft. copper).

## TAPE AND REEL

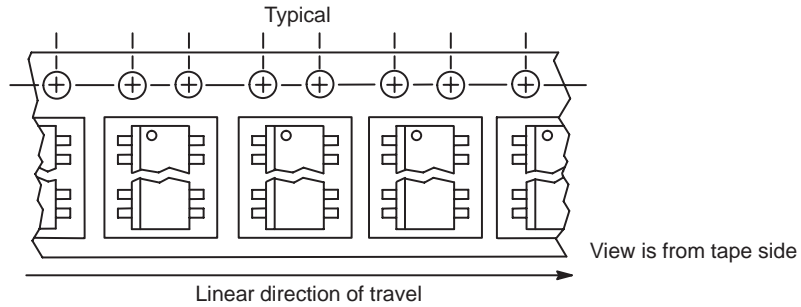
### STANDARD BIPOLAR LOGIC INTEGRATED CIRCUITS

ON Semiconductor has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms

to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

### MECHANICAL POLARIZATION

#### SOIC DEVICES



#### GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix R2
- Tape Width 12 mm to 24 mm (see table)
- Units/Reel (see table)
- No Partial Reel Counts Available and Minimum Lot Size is Per Table

#### ORDERING INFORMATION

To order devices which are to be delivered in Tape and Reel, add the suffix R2 to the device number being ordered.

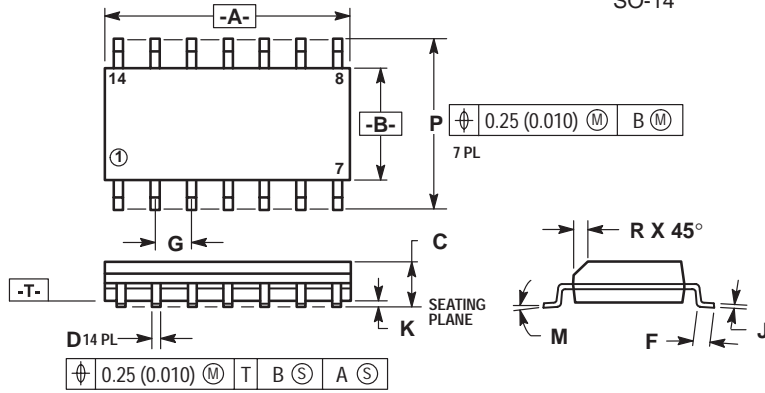
**Table 1**  
**Tape and Reel Data**

Device Type	Tape Width (mm)	Device/Reel	Reel Size (inch)	Min Lot Size Per Part No. Tape and Reel
SO-8	12	2,500	13	5,000
SO-14	16	2,500	13	5,000
SO-16	16	2,500	13	5,000
SO-16 Wide	16	1,000	13	5,000
SO-20 Wide	24	1,000	13	5,000

# PACKAGE OUTLINES

## SOIC

### Case 751A-02 D Suffix 14-Pin Plastic SO-14

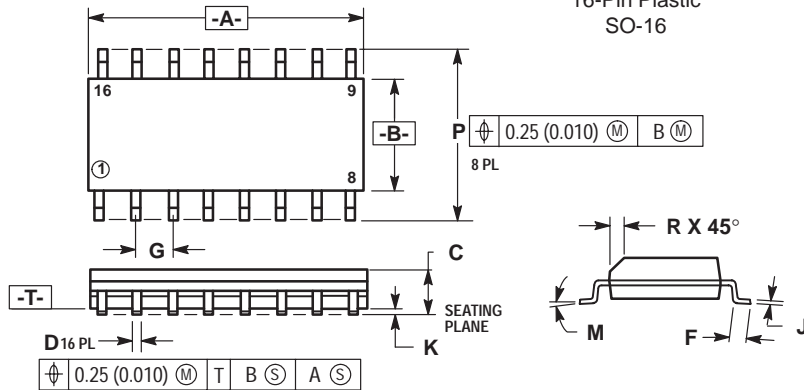


#### NOTES:

1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### Case 751B-03 D Suffix 16-Pin Plastic SO-16

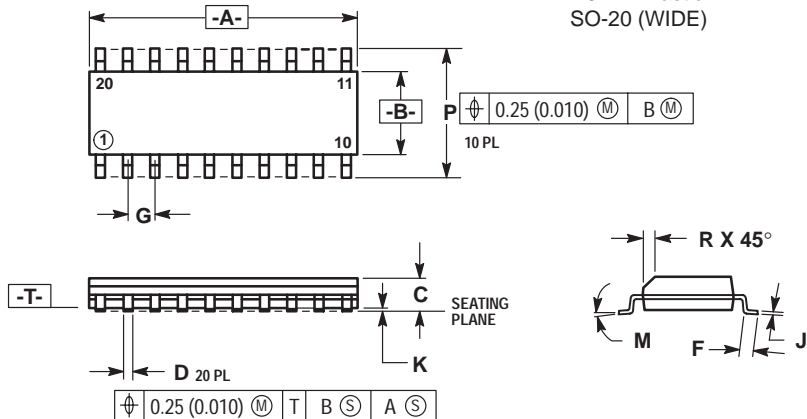


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### Case 751D-03 DW Suffix 20-Pin Plastic SO-20 (WIDE)



#### NOTES:

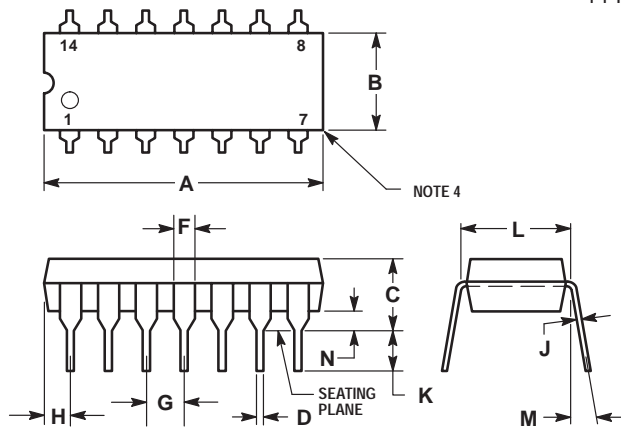
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

# PACKAGE OUTLINES

## PLASTIC

Case 646-06  
N Suffix  
14-Pin Plastic



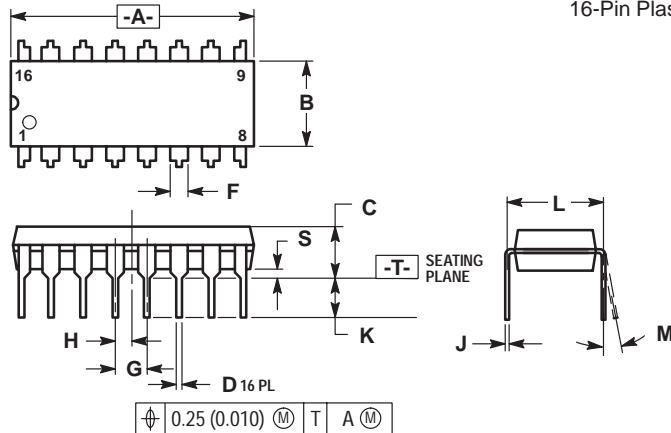
NOTE 4

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

Case 648-08  
N Suffix  
16-Pin Plastic

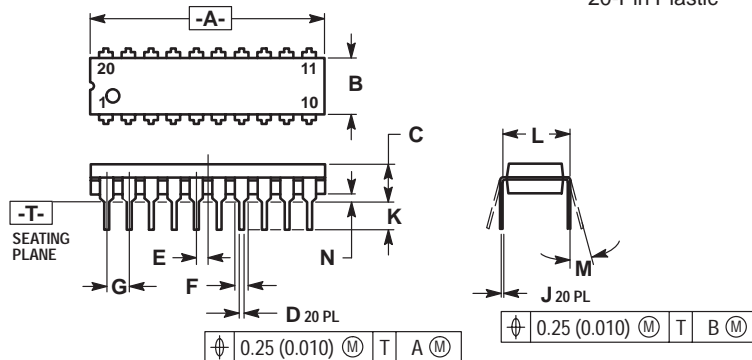


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 738-03  
N Suffix  
20-Pin Plastic



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

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## ON SEMICONDUCTOR STANDARD DOCUMENT TYPE DEFINITIONS

### REFERENCE MANUAL

A Reference Manual is a publication that contains a comprehensive system or device-specific description of the structure and function (operation) of a particular part/system; used overwhelmingly to describe the functionality of a microprocessor, microcontroller, or some other sub-micron sized device. Procedural information in a Reference Manual is limited to less than 40 percent (usually much less).

### USER'S GUIDE

A User's Guide contains procedural, task-oriented instructions for using or running a device or product. A User's Guide differs from a Reference Manual in the following respects:

- \* Majority of information (> 60%) is procedural, not functional, in nature
- \* Volume of information is typically less than for Reference Manuals
- \* Usually written more in active voice, using second-person singular (you) than is found in Reference Manuals
- \* May contain photographs and detailed line drawings rather than simple illustrations that are often found in Reference Manuals

### POCKET GUIDE

A Pocket Guide is a pocket-sized document that contains technical reference information. Types of information commonly found in pocket guides include block diagrams, pinouts, alphabetized instruction set, alphabetized registers, alphabetized third-party vendors and their products, etc.

### ADDENDUM

A documentation Addendum is a supplemental publication that contains missing information or replaces preliminary information in the primary publication it supports. Individual addendum items are published cumulatively. Addendums end with the next revision of the primary document.

### APPLICATION NOTE

An Application Note is a document that contains real-world application information about how a specific ON Semiconductor device/product is used with other ON Semiconductor or vendor parts/software to address a particular technical issue. Parts and/or software must already exist and be available.

A document called "Application-Specific Information" is not the same as an Application Note.

### SELECTOR GUIDE

A Selector Guide is a tri-fold (or larger) document published on a regular basis (usually quarterly) by many, if not all, divisions, that contains key line-item, device-specific information for particular product families. Some Selector Guides are published in book format and contain previously published information.

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# Notes



# Notes

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